Temperature characteristics of Gate all around nanowire channel Si-TFET

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Firas Natheer Abdul-kadir Agha[1], Yasir Hashim[2,*], Waheb Abduljabbar Shaif Abdullah[3]

[1]Department of Electrical Engineering, College of Engineering, University of Mosul, Mosul, Iraq

[2]Department of Computer Engineering, Faculty of Engineering, Tishk International University, Erbil-Kurdistan, Iraq

[3]Faculty of Electrical & Electronics Engineering Technology, Universiti Malaysia Pahan, 26600 Pekan, Pahang Darul Makmur, Malaysia

*yasir.hashim@ieee.org

Abstract. This paper study the impact of working temperature on the electrical characteristics of gate all around nanowire channel Si-TFET and examines the effect of working temperature on threshold voltage, transcondactance (gm), I_{ON}/I_{OFF} ratio, drain induced barrier lowering (DIBL), and sub-threshold swing (SS). The (Silvaco) simulation tool has been used to investigate the working temperature on the Si-TFET characteristics. The temperature range in this study is from -25 to 150 ^{o}C. The results indicate that the TFET must work in electronic circuits with the lower temperature as possible to get better performances. Furthermore, the TFET has good performances as a temperature nanosensor with diode connection mode under ON conditions.

1. Introduction

In nanotechnology regime, The nanowire Tunnel Field Effect Transistors (TFET) are good alternatives to replace the existing Metal Oxide Semiconductor Field Effect Transistor (MOSFET) and it has a potential candidate for electronic devices, because the TFET have low OFF current (I_{OFF}), small sub-threshold swing (less than 60 mV/decade), low power consumption and reduced Short Channel Effects (SCE) [1-5].

The physical mechanics of tunnel field effect transistor TFET is using quantum band-to-band tunneling effect (BTBT) to transport carriers from a valence band of Source (P) to a valance band of Drain (D) through the channel or Gate (G) which is totally different from conventional MOSFET devices that use thermionic emission as shown in Figure1[6-10]. There are two models for tunneling mechanism, local and non-local tunneling model, the non-local model can be considered very important model in the designing of TFET because it keeps sub-threshold swing up to 60 mV/decade [11]. Since the current in the TFETs is done by the valence band of the source that comprise lower energy the TFETs are considered thermally cooled regime and the SS are not anticipated to be limited

by the temperature. On the other hand, in the case of ON current (I_{ON}) for the device, the applied voltage at the gate (V_{GS}) will pulls back the energy band of the channel area and decrease the height of the barrier. Subsequently the carriers will tunnel from source to channel regions and hence the tunneling current will constitute [10].

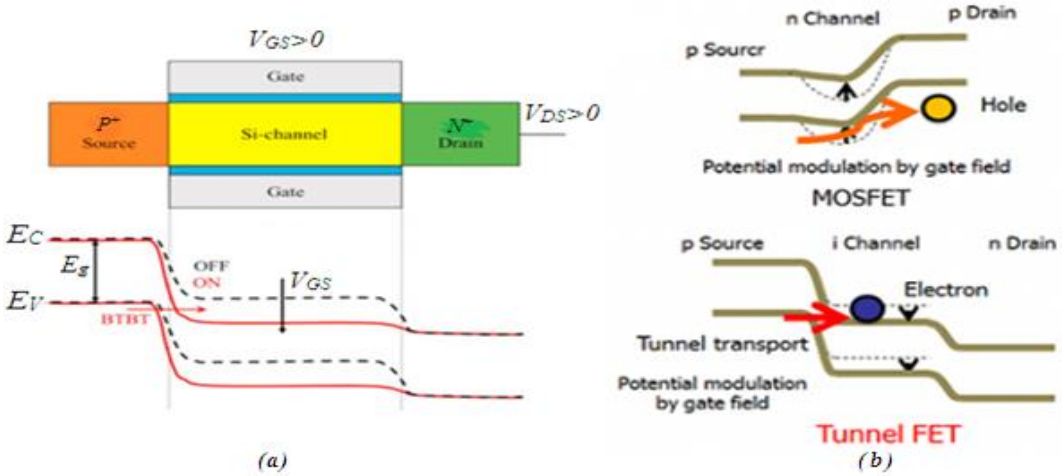

Fig. 1. (a) Schematic of a TFET cross section and band diagram along the channel in ON and OFF states, (b) Comparison between TEFET and MOSFET according to operation principle (b).

The basic structure of a TFET is consist of three region (P-I-N), where source is highly doped with (P+) type, channel is intrinsic doped (I) and drain is highly doped with (N^+) type and oxide layer is surround the Si-channel as shown in Figure1.a [12]. A positive voltage is applied at the drain and gate terminals, and biases is reversed between source-channel and drain-channel. TFET fabricated in different types of topologies, depending upon tunneling junction electric field and gate electric field.

There are two most important types of topologies used in fabricated TFET:

1. Lateral Tunnel Field Effect Transistor (LTFET).
2. Vertical Tunnel Field Effect Transistor (VTFET).

But vertical TFETs have a smaller OFF state current and have a steeper sub-threshold swing as compared to lateral counterparts [13-14]. Surround gate or GAA structure as shown in Figure 2 permits more channel width per unit area of silicon nanowire [15].

2. Methodology

A gate all around TFET device has been designed and simulated by using Silvaco program by the specified dimension of nanometers scales. Figure 3 shows a cross-sectional area of the geometric structure and limited dimension of the device. Where the radius of the silicon intrinsic channel is (R), the gate length (L_G) and thickness of the gate oxide dielectric material SiO2 is (T_{ox}).

Doping concentration of the channel is 10^{17} per cm^{-3} and doping concentrations for drain and source is 10^{19} per cm^{-3} respectively. The dimensions of the channel L_G is 200 nm, radius of the channel R is 35nm, SiO_2 thickness T_{ox} is 4.5 nm and dimensions for drain and source lengths (L_S and L_D) is 80 nm respectively, other parameters illustrated in Table 1.

In this work, we used various temperature degrees, from -50°C to 150°C step-up by 25°C. The voltage taken at the drain terminal (V_{DS}) is 1v and voltage applied at the gate terminal (VGS) is varied from 0v to 1v in step-up 0.1v. Various parameters and characteristics of GAA Si TFET are investigated and verified using Silvaco. Some of these parameters are I_{ON}/I_{OFF}, SS, DIBL (Drain Induced Barrier Lowering) and transconductance (g_m), where the drain current I_D of a TFET, it dependence on the temperature degree according to the following equation [16]:

$$I_D = A \cdot {V_{Gs}}^2 \cdot \ exp\left(-\frac{B}{V_{GS}}\right) \text{ ..... (1)}$$

$$A \propto {E_G}^{-0.5}$$

$$B \propto {E_G}^{1.5}$$

A and B are carrier effective mass and tunneling barrier

A relationship between the variations of the energy gap (Eg) with temperature (T) in semiconductors is proposed as [17]:

$$E_G = E_0 - \alpha T^2/(T+\beta) \text{ .....(2)}$$

Where α and β are constants.

As temperature decreases, the EG increases, leading to parameter B will increase and hence a decreasing tunneling current (I_D). Also, the sub- threshold swing SS dependence upon the temperature degree as following equation [18]:

$$SS \cong \left(1 + \frac{C_d}{C_{ox}}\right) ln \frac{KT}{q} \text{ .....(3)}$$

Finally, the transconductance (g_m) will increased when ID increases as proposed as [18]:

$$g_m = \frac{\partial I_D}{\partial V_{GS}} \text{ .....(4)}$$

So, the temperature effect is dominated on performance of the TFETs due to the temperature variation of the band gap (EG). The important of this work lies in achieving low SS, low OFF state current, increase I_{ON}/I_{OFF} and increase gm at low-temperature degree.

Table- I: Parameters of simulated TFET

Parameter	Value
Channel radius (R)	(35) nm
Oxide thickness (T_{OX})	(4.5) nm
Channel Doping (P)	10^{17} cm^{-3}
Drain Doping (P^+)	10^{19} cm^{-3}
Source Doping (N^+)	10^{19} cm^{-3}
Drain length	80 nm
Source length	80nm
Channel length (L)	(200) nm

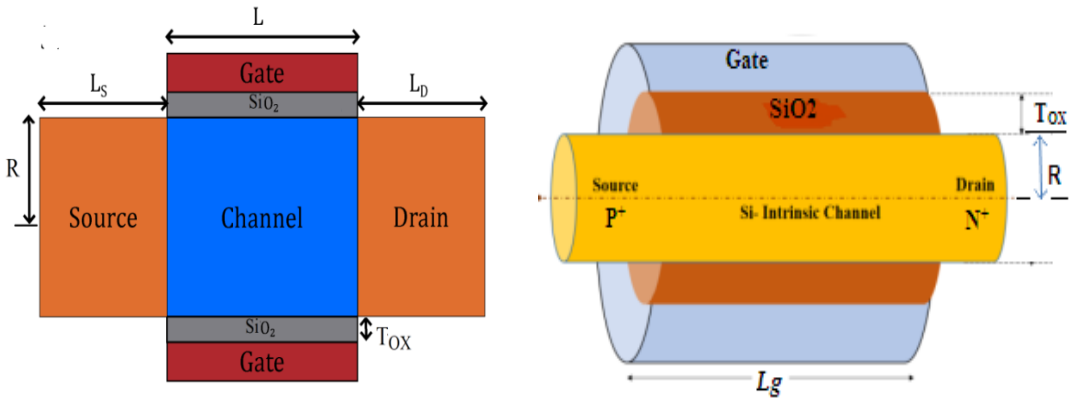

Fig. 2. GAA Si TFET structure

3. Results and Discussion

Figure 3 illustrates the dependence of threshold voltage on working temperature and the V_T decreases linearly with increasing working temperature. Figure 4 shows the variation of transconductance channel (g_m) of TFET with working temperature, the gm decreases exponentially with increasing working temperature.

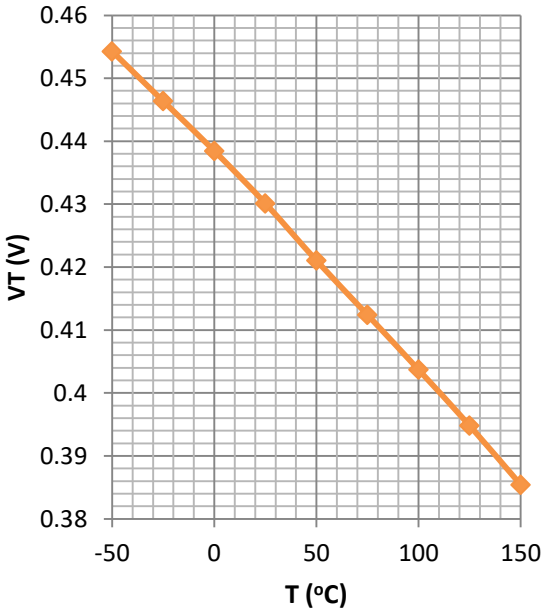

Fig. 3. The dependence of threshold voltage on working temperature

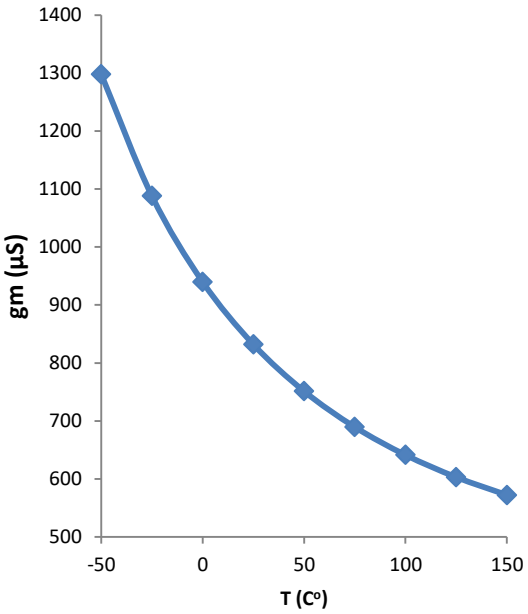

Fig. 4. The variation of transconductance channel (g_m) of TFET with working temperature.

Figure 5 illustrates the impact of working temperature on drain ON to OFF current (I_{ON}/I_{OFF}) ratio, which considered is one of the most significant parameters for using transistors in digital electronic circuits. According to Figure 5, the maximum ratio of I_{ON}/I_{OFF} occurs at -25 ^{o}C and then exponentially decreased. For numerous transistor applications in electronic circuit such as logic gates and amplifiers, the highest value of I_{ON}/I_{OFF} current ratio is the best for these applications. So, the findings of ON to OFF drain current ratio (I_{ON}/I_{OFF}) with temperature characteristics may lead to use of TFET in electronic circuits with lower temperature to obtain a higher I_{ON}/I_{OFF} ratio as possible.

Figure 6 illustrates the change in subthreshold swing (SS) with working temperature. SS mathematically is known as the slope inverse of the transfer characteristics (I_d versus V_g) curve under condition that the Id in a logarithmic scale. Depending on this figure, SS increases near to be linearly with increasing environmental temperature. The minimum SS value is at -50 ^{o}C, and it is possible to define it as a best SS. It is clear that all SS values much under the ideal value of SS in normal MOSFET (60 mV/dec). The outcome of SS with working temperature might drive to the use of TFET in switching circuits with minimum temperature as possible to get lower SS and then faster switching operation.

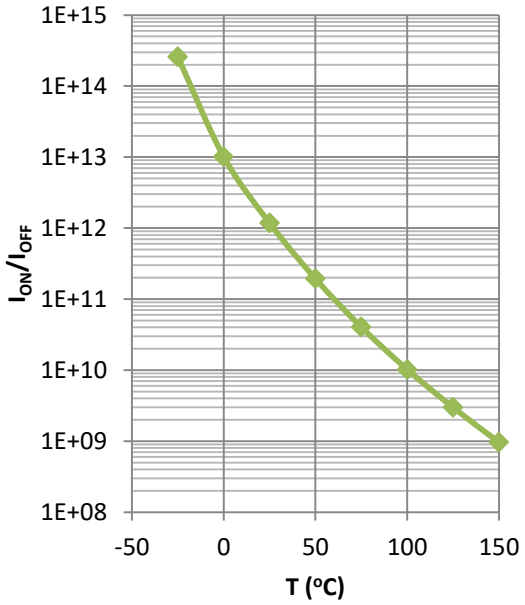

Fig. 5. The impact of working temperature on (I_{ON}/I_{OFF}) ratio.

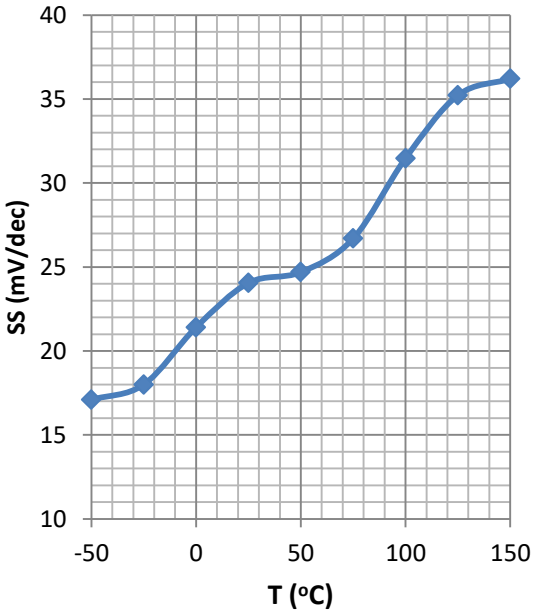

Fig. 6. The subthreshold swing (SS) with working temperature characteristics.

Drain induced barrier lowering (DIBL) is one of the important key parameters for test and evaluate the performances of FET structures. DIBL varied depending on environmental temperature of TFET, as shown in Fig. 7, which increases linearly as environmental temperature increases from -50 °C to 150 °C. So, the raise in working temperature has a serious effect on DIBL, making the TFET works with poor performances in electronic circuits.

Figure 8 shows the temperature sensitivity of both OFF and ON currents with increasing environmental temperature. The evaluation of TFET as a temperature nanosensor is possible based on this figure. The OFF current temperature sensitivity ($I_{OFF}/\Delta T$) increases exponentially with increasing environmental temperature, and the maximum value is 2.94×10^{-16} A/°C, while, the temperature sensitivity of ON current ($I_{ON}/\Delta T$) increases linearly with increasing environmental temperature, and the maximum value is 6.26×10^{-9} A/°C. It is clear that the I_{ON} current has the higher temperature sensitivity and it is the suitable current for using the TFET as a temperature nanosensor. MOSFET structure can be used as a temperature sensor by connecting the diode mode by connecting the gate with drain (circuit in Figure 9). Fig. 9 shows the increment of current ΔI with increasing environmental temperature at $V_g = V_{DS} = V_{DD}$=1V, the ΔI increased linearly with temperature, so, the TFET has a good performances as a temperature nanosensor.

Finally, the importance impact of working temperature on I_D in TFET could be referring to the higher carrier velocity for n-type NWs as the radius minimized [19]. Furthermore, in highly FETs scaled-down, the saturation current of drain is controlled by the effective carrier injection velocity (V_{inj}) from the source to the channel. The ballistic transport does not depends on the concept of mobility, and the controlling of current will depends on the carrier injection velocity, that is a semiconductors material features.

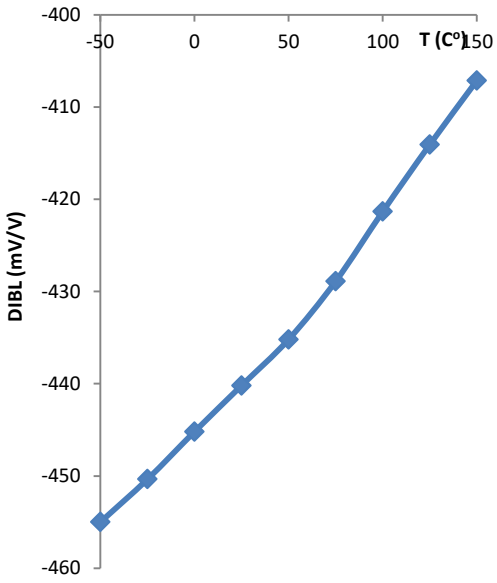

Fig. 7. The DIBL with working temperature characteristics.

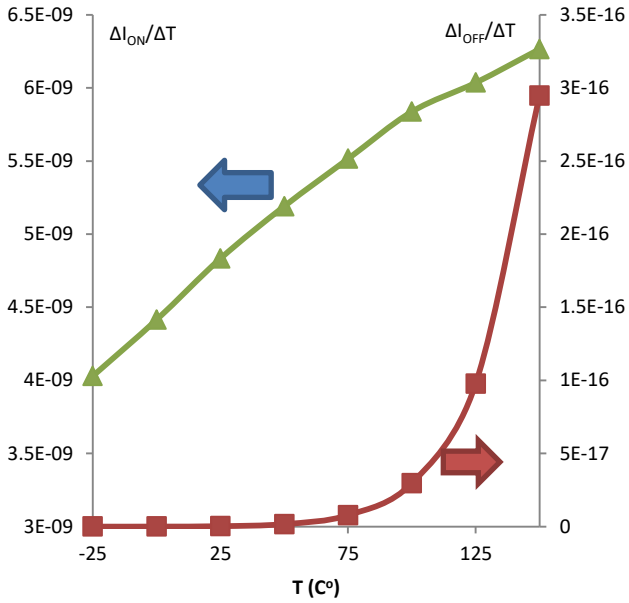

Fig. 8. The temperature sensitivity of both OFF and ON currents with increasing environmental temperature.

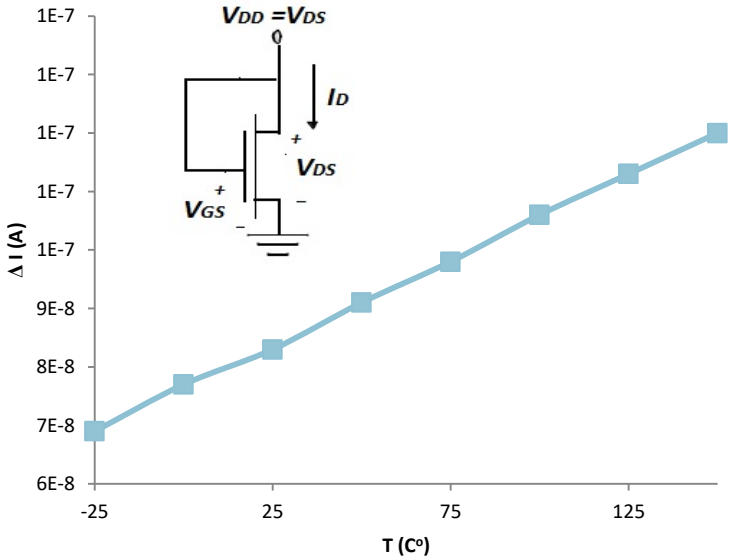

Fig. 9. The increment of current ΔI with increasing environmental temperature at Vg = V_{DS} = V_{DD}=1V.

4. Conclusion

This paper presents the investigation of environmental temperature characteristics of TFET. Silvaco simulation tool has been used in this investigation. The findings of V_T, g_m, I_{ON}/I_{OFF}, SS, and DIBL with working temperature indicate that the TFET must work in electronic circuits with the lower temperature as possible to get better and lower SS and DIBL with higher I_{ON}/I_{OFF} ratio. Furthermore, the using of TFET as a temperature nanosensor must happen under the ON conditions because of the higher ON current temperature sensitivity ($I_{ON}/\Delta T$), the TFET has good performances as a temperature nanosensor with diode connection mode.

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