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Combined (Si) and (Ge) FinFET-CMOS Inverter Characterization Based on Driver to Load Transistor Ratio

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This paper proposes a novel method to adaptively select the best driver to load transistor fin ratio of CMOS FinFET logic inverter according to the best values of noise margins and inflection voltage with a comparison of the use of different and combined Si and Ge as a load and/or driver semiconductor channel in CMOS FinFET inverter logic circuit. The methodology of optimizing the driver to load transistor fin ratio depends strongly on improving the noise margins and inflection voltage of the output characteristics of CMOS logic inverter. The first step in this investigation of CMOS-FinFET-inverter is to obtain the output characteristics (I_d-V_d) of the FinFET, and then use the MATLAB simulation model to create CMOS FinFET transfer characteristics. Transfer characteristics of CMOS-FinFET-logic inverter are studied with fin ratios N_p/N_n of 5/1, 4/1, 3/1,2/1, 1/1, 1/2, 1/3, 1/4, 1/5. Noise margins and inflection voltage are used as critical factors to obtain the optimal fin ratio (N_p/N_n). The results indicate that optimization depends strongly on the fin ratio for all combined semiconductor loads to FinFET driver inverters. The results show that the best ratios for Si:Si, Si:Ge, Ge:Si, and G:Ge are 2:1, 1:4, 2:1, and 1:3 respectively.

Keywords: FinFET, CMOS, Transistor, Inverter, Transfer characteristics.

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1. INTRODUCTION

As the traditional structure of silicon Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) has very near to its minimization limits, many new structures are investigated extensively. FinFET is one of these new nanoscale structures. FinFET is of great interest both for researchers and for the semiconductor industry [1].

Transistors in nanoscale, like Silicon Nanowire Transistors (SiNWTs), Carbon Nanotube Transistors (CNTs) and FinFETs, generate significant interest from the industry of electronic devices because of the leadership in minimal, reliable and faster electronic devices. The functionality of a new generation of nanodimensional circuits and a broadband range of extra applications depends on studying the characteristics of these devices [2]. These new versions of MOSFETs and higher speed Integrated Circuits (ICs) using new semiconductor nanodimensional structures with a fin-like channel will have many applications in the near future after intensive investigation of their characteristics by researchers. The manufacturing technologies of ICs based on FinFETs are still in the growth phase, that demands more invention together with the confronting state-of-the-art MOSFETs.

To grasp the characteristics of FinFET in depth, and also to evaluate its performances, the simulation became an important and the leader of this new technology. Moreover, simulation work could be supported by the experimental work to speed up the improvements of FinFETs by reducing their cost, determining their weakness and strength, and minimizing their dimensions down to the nanometers zone [3-5].

According to the 2016 road map ITRS 2.0, FinFET will be the dominant future transistor in CMOS technology because of its ability to continue scaling down to 5 nm node technology and beyond [6], because its fin-shaped channel, which tends to superior gate control, then enables many improvements of short channel effects in planner MOSFET, like improved subthreshold slope and higher I_{ON}/I_{OFF} ratio [7, 8]. The perfect gate design with low OFF state leakage current tends to adoption of FinFET for high-volume ICs production with 22 nm node technology generation [9].

Neha et. al. [10] explored Ge-FinFET under scaling the germanium fin with standard cell architectures at the node of sub 5 nm. Neha et. al. [10] explained that the germanium device has almost 70 % improvement in drive current and 3.4× less in resistance device.

This paper proposes a novel method to adaptively select the best driver to load transistor fin ratio (N_p/N_n) of CMOS inverter with combined (Si) and (Ge-) FinFET load and driver transistors, where N_p is the number of fins of driver n-channel transistor and N_n is the number of fins of load p-channel transistor. The best value of the fin ratio (N_p/N_n) of FinFET-SRAMs will be found according to the best values of noise margins and inflection voltages with a comparison between using Si and Ge as semiconductor channel in FinFET-CMOS inverter.

Fig. 1 illustrates the most commonly used FinFET architecture, the most accurate configuration content of CMOS inverter unit is shown in Fig. 2. The n-channel transistor is the driver transistor, and the p-channel transistor as the load transistor.

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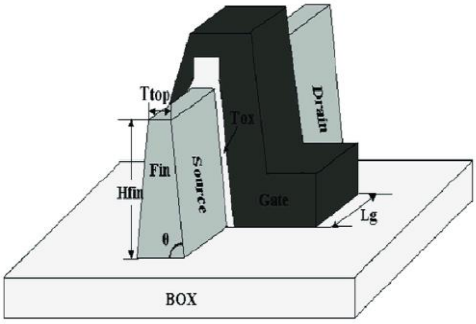

Fig. 1 – FinFET structure

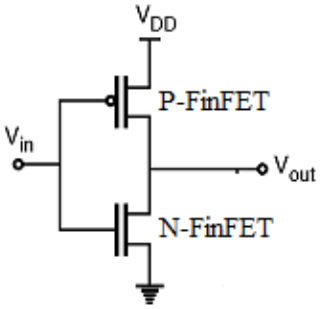

Fig. 2 – CMOS-FinFET inverter

2. METHODOLOGY

The first step of this investigation of the FinFET-CMOS inverter is producing the output characteristics (I_D-V_D) of FinFET. In this research, the output characteristic (I_D-V_D) of FinFET is simulated using a simulation tool (MUGFET) [11]. The MUGFET simulation software tool is invented at Purdue University. Table 1 illustrates parameters that are used in this simulation step to find the output characteristics of FinFET.

Fig. 3 represents the output characteristics of load (p-channel) and driver (n-channel) transistors that are produced by MUGFET, these results are used as a data file for the second step of simulation.

The second step in this investigation of the FinFET-CMOS inverter characteristics is using a new MATLAB model (proposed in [12]) to produce the transfer characteristics of the CMOS inverter. This model is used to produce the transfer characteristics of FinFET logic inverter. The model is designed to find the intersection points of curves having the same gate voltage of the load (I_D-V_D) and driver FinFET that is configured as a CMOS inverter circuit.

Mainly, the MATLAB model is constructed to produce the V_{out}-V_{in} and I_{out}-V_{in} characteristics of the Fin-FET-CMOS inverter circuit based on the output characteristics of FinFET [12]. This new model will calculate low (NM_L) and high (NM_H) noise margins. The fin ratio optimization in principle will be based on improving the inflection voltage (V_{inf}) and noise margins. The low and high noise margins and inflection voltage are used as limiting factors in this study. So, the best inverter is the one that has equal and higher values as possible of noise margins (NM_H) and (NM_L). Both NM_H and NM_L must have higher values and equal as possible, and the V_{inf} value must be near to the half of V_{dd}.

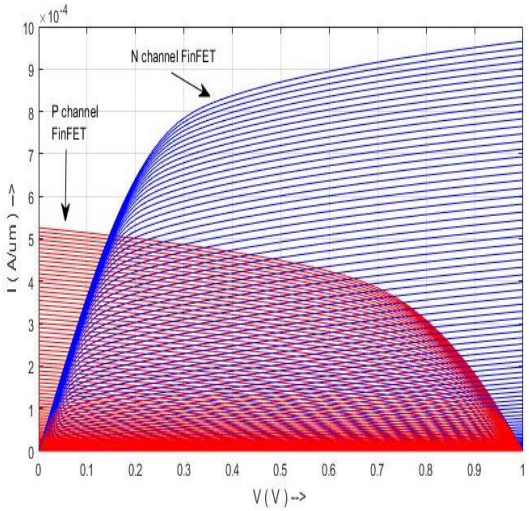

Fig. 3 – Output characteristics of load (p-channel) and driver (n-channel) transistors

Table 1 – Parameters of FinFET

Parameter Name	*n*-channel	*p*-channel
Fin width (T)	30 nm	30 nm
Source length	50 nm	50 nm
Drain length	50 nm	50 nm
Channel length (L_g)	45 nm	45 nm
Oxide thinness (SiO_2) (Tox)	2.5 nm	2.5 nm
Gate overlap	2 nm	2 nm
Channel concentration	$1{\cdot}10^{16}$/cm^3 (p-type)	$1{\cdot}10^{16}$/cm^3 (n-type)
Source and drain concentration	$1{\cdot}10^{19}$/cm^3 (n-type)	$1{\cdot}10^{19}$/cm^3 (p-type)

3. RESULTS AND DISSCUSION

Fig. 4 presents the output characteristics of CMOS inverters based on Si-FinFET for both load and driver transistors. According to these characteristics, the fin ratio of driver to load FinFET with 1/1 provides an acceptable characteristic depending on $NM_L = 0.28$, $NM_H = 0.408$ and $V_{inf} = 0.44$, but it was improved by increasing N_p/N_n to 2/1 because of both noise margins are almost equal, and both are nearer to the inflection voltage. $NM_L = 0.34$, $NM_H = 0.35$ and $V_{inf} = 0.49$ according to this condition, while the characteristics are worse if N_p/N_n is increased by more than 2/1 or N_n/N_p is increased by whatever ratio.

The current characteristics of CMOS inverters based on load and driver Si- FinFET are explained in Fig. 5. The current characteristics illustrate that the current always increases with increasing N_p/N_n or N_n/N_p, but the inflection voltage shifts in the opposite direction for both conditions.

Fig. 5 explains how the ratio of N_p/N_n affects the total current passing through both transistors (load and driver), and this will affect the inflection point that occurs at the peak of the current curve. It is possible to recognize that the best characteristics are obtained when the inflection point falls on the mid value of V_{in}, in Fig. 4, at $N_p/N_n = 2/1$.

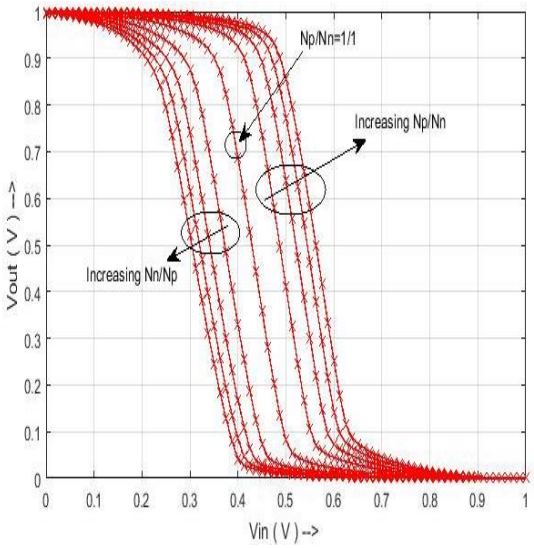

Fig. 4 – Transfer characteristics of Si:Si CMOS logic inverter with changing N_p/N_n = 5/1, 4/1, 3/1,2/1, 1/1, 1/2, 1/3, 1/4, 1/5

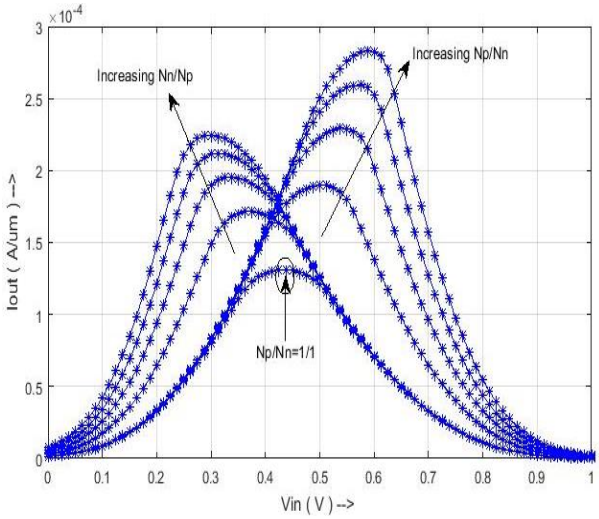

Fig. 5 – Current characteristics of Si:Si CMOS logic inverter with changing N_p/N_n = 5/1, 4/1, 3/1,2/1, 1/1, 1/2, 1/3, 1/4, 1/5

Fig. 6 shows the noise margins and inflection voltage variation with the N_p/N_n fin ratio, the intersection point of NM_H and NM_L is obtained at 2/1 fin ratio, and this actually represents the best and optimized value as a working point for the logic inverter, and the increase in N_p/N_n will present worse working conditions because NM_L and NM_H are not equal, and NM_H will be very low as it is far from the inflection voltage. On the other hand, increasing N_n/N_p (decreasing N_p/N_n) will have the opposite effect, meaning that NM_L will be very low and farer from the inflection voltage, and will also create bad working conditions for the CMOS inverter.

Fig. 7 illustrates the transfer characteristics of CMOS logic inverter with Ge-FinFET as a load and driver *n*-channel and *p*-channel transistors respectively and at fin ratio of N_p/N_n = 5/1, 4/1, 3/1,2/1, 1/1, 1/2, 1/3, 1/4, and 1/5. It is clear that from this figure, the best characteristics occur at N_p/N_n = 1/3, meaning that this inverter needs 3 fins of *p*-channel driver Ge-FinFET with 1 fin of *n*-channel load Ge-FinFET to improve the characteristics of CMOS logic inverter with Ge-FinFET, while the characteristics will deteriorate with increasing N_p/N_n or N_n/N_p ratio more than 3/1.

Fig. 8 presents the current characteristics of the same inverter circuit with the variation of N_p/N_n fin ratio. The current increases with increasing either N_p/N_n or N_n/N_p, but the inflection voltage is improved significantly at N_n/N_p = 3/1. Fig. 8 illustrates that the ratio of N_p/N_n affect the total current passing through both transistors (load and driver) and this will affect the inflection point that occurs at the peak of the current curve. It is possible to recognize that the best characteristics are obtained when the inflection point occurs near the mid value of V_{in} at N_p/N_n = 3/1.

Fig. 9 results the noise margins (NM_H and NM_L) and inflection voltage variation with N_p/N_n. It is clear that the best and optimized point is at N_p/N_n = 3/1, which occurs at $NM_H = NM_L$. The best and optimized values for noise margins are NM_H = 0.27 V and NM_L = 0.31 V, where the inflection voltage is 0.53 V.

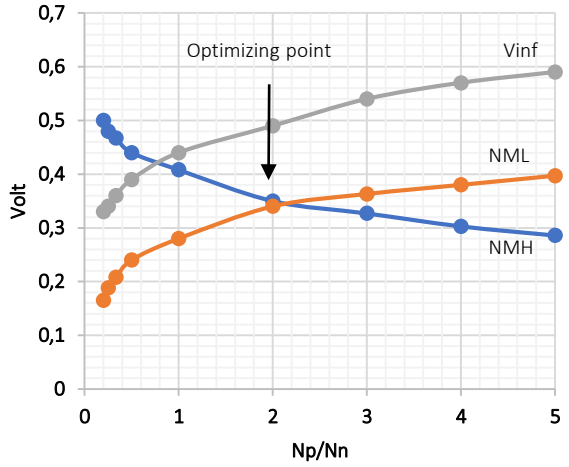

Fig. 6 – Noise margins and inflection voltage variation with N_p/N_n fin ratio of Si:Si CMOS logic inverter

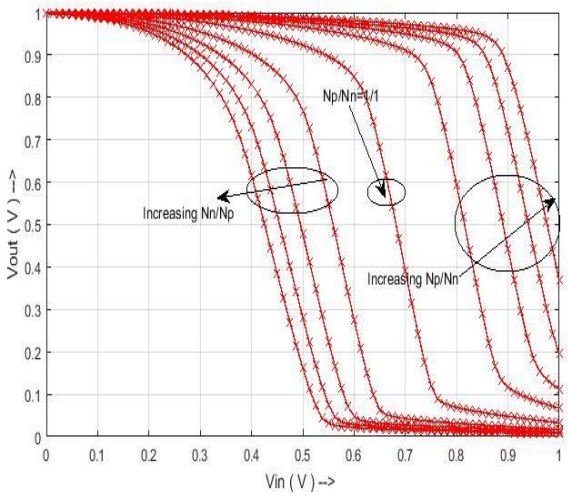

Fig. 7 – Transfer characteristics of Ge:Ge CMOS logic inverter with changing N_p/N_n = 5/1, 4/1, 3/1,2/1, 1/1, 1/2, 1/3, 1/4, 1/5

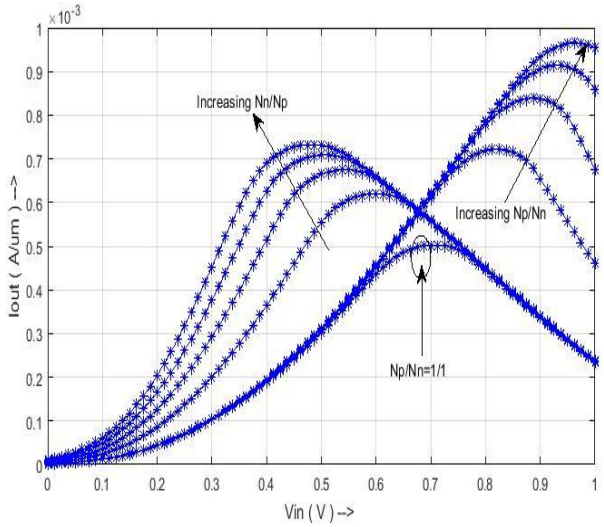

Fig. 8 – Current characteristics of Ge:Ge CMOS logic inverter with changing N_p/N_n = 5/1, 4/1, 3/1,2/1, 1/1, 1/2, 1/3, 1/4, 1/5

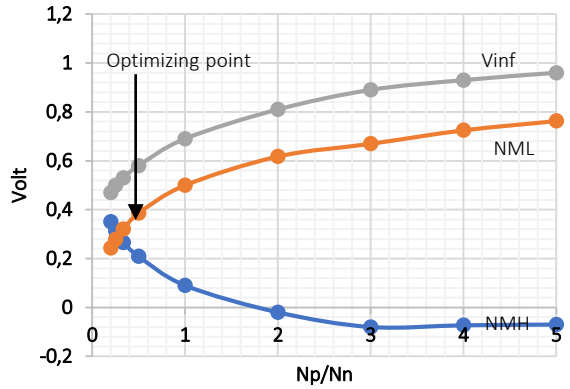

Fig. 9 – The noise margins and inflection voltage variation with the N_p/N_n fin ratio of Ge:Ge CMOS logic inverter

Fig. 10 shows the transfer characteristics of CMOS logic inverter with Si-FinFET as a load *p*-channel transistor and Ge-FinFET as a driver *n*-channel transistor and at the fin ratio of N_p/N_n = 5/1, 4/1, 3/1,2/1, 1/1, 1/2, 1/3, 1/4, and 1/5. It is seen from this figure that the best characteristics are at N_p/N_n = 1/4, meaning that this inverter needs 4 fins of *n*-channel driver Ge-FinFET with 1 fin of *p*-channel load Si-FinFET to improve the characteristics of Si:Ge FinFET CMOS logic inverter, while the characteristics will deteriorate as the N_p/N_n ratio or N_n/N_p ratio increase more than 4/1.

Fig. 11 presents the current characteristics of the same inverter circuit with the variation of the fin ratio N_p/N_n. The current increases with increasing either N_p/N_n or N_n/N_p, but the inflection voltage is improved significantly at N_n/N_p = 4/1. Fig. 11 explains the effect of N_p/N_n on the total current passing through both transistors (load and driver), and this will affect the inflection point that is at the peak of the current curve. It is clear that the best inflection point occurs near the mean value of V_{in}, at N_p/N_n = 4/1.

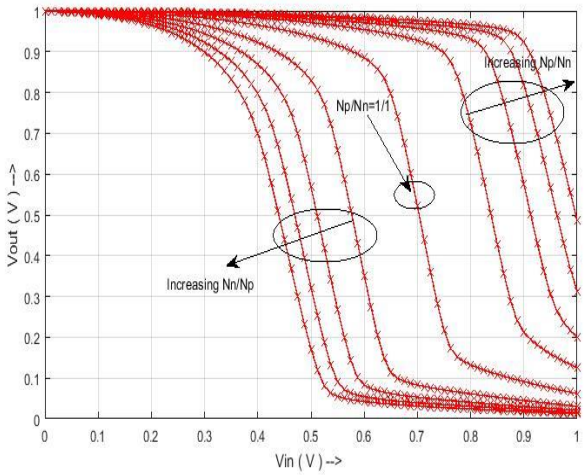

Fig. 10 – Transfer characteristics of Si:Ge CMOS logic inverter with changing N_p/N_n = 5/1, 4/1, 3/1,2/1, 1/1, 1/2, 1/3, 1/4, 1/5

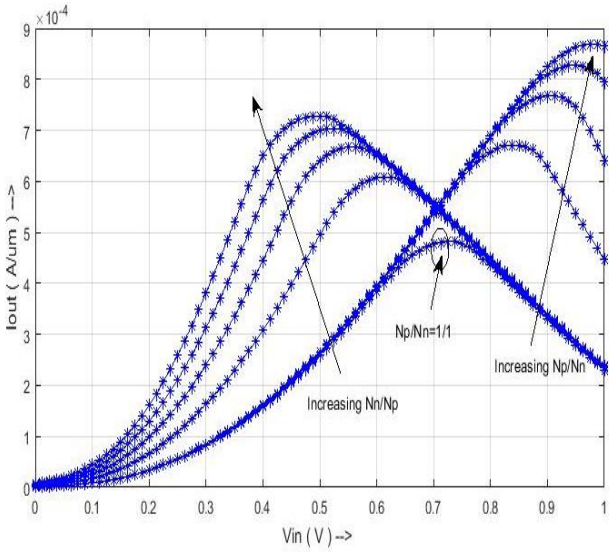

Fig. 11 – Current characteristics of Si:Ge CMOS logic inverter with changing N_p/N_n = 5/1, 4/1, 3/1,2/1, 1/1, 1/2, 1/3, 1/4, 1/5

Fig. 12 results the noise margins (NM_H and NM_L) and inflection voltage variation with N_p/N_n. It is clear that the best and optimized point is at N_p/N_n = 1/4, which occurs at $NM_H = NM_L$. The best and optimized values for the noise margins are NM_H = 0.315 V and NM_L = 0.275 V, when the inflection voltage is 0.5 V.

Fig. 13 explains the transfer characteristics of CMOS logic inverter with Ge-FinFET as a load *p*-channel transistor and Si-FinFET as a driver *n*-channel transistor and at the fin ratio of N_p/N_n = 5/1, 4/1, 3/1,2/1, 1/1, 1/2, 1/3, 1/4, and 1/5. It is seen from this figure that the best characteristics occur at N_p/N_n = 2/1, meaning that this inverter needs 2 fins of *p*-channel load Ge-FinFET with 1 fin of *n*-channel driver Si-FinFET to improve characteristics of Ge:Si FinFET CMOS logic inverter, while the characteristics will deteriorate with increasing N_p/N_n or N_n/N_p ratios more than 1/2.

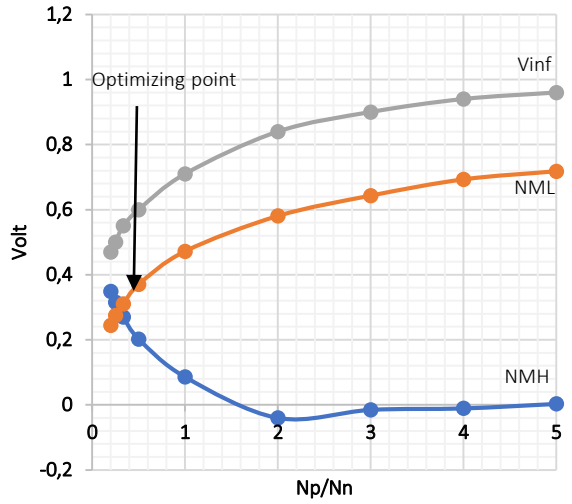

Fig. 12 – Noise margins and inflection voltage variation of Si:Ge CMOS logic inverter with changing N_p/N_n = 5/1, 4/1, 3/1, 2/1, 1/1, 1/2, 1/3, 1/4, 1/5

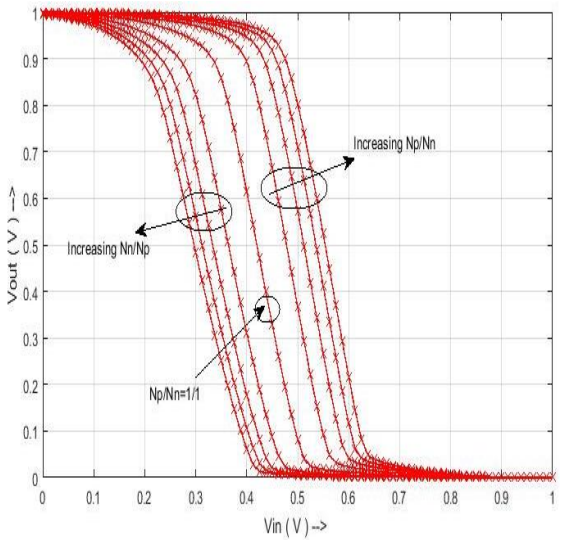

Fig. 13 – Transfer characteristics of Ge:Si CMOS logic inverter with changing N_p/N_n = 5/1, 4/1, 3/1,2/1, 1/1, 1/2, 1/3, 1/4, 1/5

Fig. 14 presents the current characteristics of the same inverter circuit with the variation of the fin ratio N_p/N_n. The current increases with increasing either N_p/N_n or N_n/N_p, but the inflection voltage is improved significantly at N_n/N_p = 1/2.

Fig. 15 results the noise margins (NM_H and NM_L) and inflection voltage variation with N_p/N_n. It is clear that the best and optimized point is at N_p/N_n = 2/1, which occurs at $NM_H = NM_L$. The best and optimized values for the noise margins are NM_H = 0.34 V and NML = 0.34 V, when the inflection voltage is 0.46 V.

Table 2 explains the results of FinFET-CMOS inverter with different configurations of load to driver (load: driver) transistor. According to these results, the best characteristics with optimal values of MN_H, NM_L, and V_{inf} occur with Ge:Si and Si;Si FinFET CMOS logic inverter at 2/1 fin ratio, and for Ge:Ge and Si:Ge FinFET CMOS logic inverter, it has an acceptable characteristic with a fin ratio of 1/3 and 1/4, respectively.

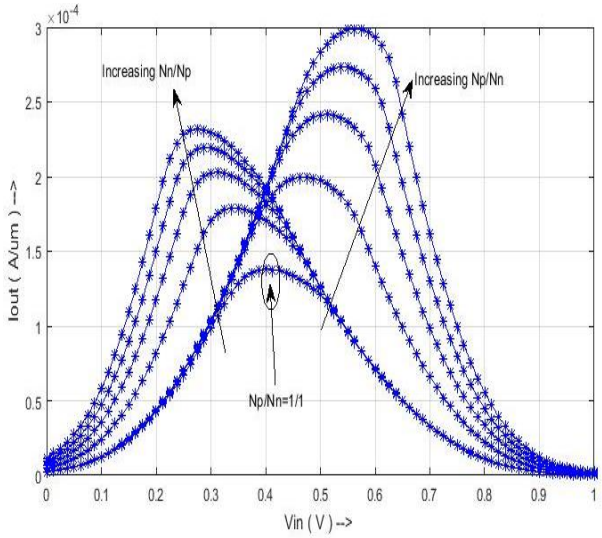

Fig. 14 – Current characteristics of Ge: Si CMOS logic inverter with changing N_p/N_n = 5/1, 4/1, 3/1,2/1, 1/1, 1/2, 1/3, 1/4, 1/5

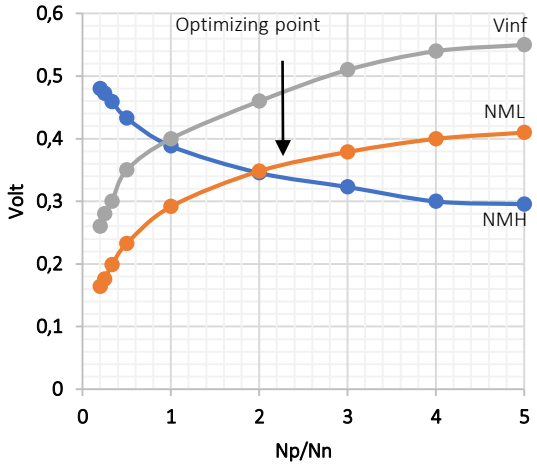

Fig. 15 – Transfer characteristics of Ge:Si CMOS logic inverter with changing N_p/N_n = 5/1, 4/1, 3/1,2/1, 1/1, 1/2, 1/3, 1/4, 1/5

Table 1 – Final results for FinFET-CMOS inverter with different configuration of load to driver (load: driver) transistors

Load: driver	Si-FinFET: Si-FinFET	Ge-FinFET: Ge-FinFET	Si-FinFET: Ge-FinFET	Ge-FinFET: Si-FinFET
Optimized N_p/N_n	2/1	1/3	1/4	2/1
Optimized NM_H	0.35	0.27	0.315	0.346
Optimized NM_L	0.34	0.31	0.275	0.348
Optimized V_{inf}	0.49	0.53	0.5	0.46

4. CONCLUSIONS

This paper proposes a novel method to select and optimize the best driver to load transistor fin ratio (N_p/N_n) of CMOS inverter with combined (Si-) and (Ge-) FinFET load and driver transistors. The results of FinFET-CMOS inverter with different configurations of load to driver (load: driver) transistor indicate that the best characteristics with optimal values of NM_H, NM_L, and

V_{inf} take place with Ge:Si and Si:Si FinFET CMOS logic inverter at 2/1 fin ratio, and for Ge:Ge and Si:GeFinFET CMOS logic inverter it has an acceptable characteristic with a fin ratio of 1/3 and 1/4, respectively.

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Характеристики комбінованого (Si та Ge) інвертора FinFET-CMOS на основі співвідношення транзисторів навантаження до драйверу

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У статті пропонується новий метод адаптивного вибору найкращого співвідношення плавців драйвера до навантажувального транзистора логічного інвертора CMOS FinFET відповідно до кращих значень запасу по шуму та напруги перегину з порівнянням при використанні комбінованих Si і Ge як навантаження та/або напівпровідникового каналу драйвера в логічній схемі інвертора CMOS FinFET. Методика оптимізації співвідношення плавців драйвера до транзистора навантаження сильно залежить від поліпшення запасу по шуму та напруги перегину вихідних характеристик логічного інвертора CMOS. Першим кроком у цьому дослідженні інвертора CMOS-FinFET є отримання вихідних характеристик (I_d-V_d) FinFET, а потім використання моделі моделювання MATLAB для створення передавальних характеристик CMOS FinFET. Досліджено передавальні характеристики логічного інвертора CMOS-FinFET із співвідношенням плавців N_p/N_n 5/1, 4/1, 3/1, 2/1, 1/1, 1/2, 1/3, 1/4, 1/5. Запаси по шуму та напруга перегину використовуються як критичні фактори для отримання оптимального співвідношення плавців (N_p/N_n). Результати показують, що оптимізація залежить від співвідношення плавців для всіх комбінованих напівпровідникових інверторів FinFET. Результати показують, що найкращі співвідношення для Si:Si, Si:Ge, Ge:Si та G:Ge становлять 2:1, 1:4, 2:1 та 1:3 відповідно.

Ключові слова: FinFET, CMOS, Транзистор, Інвертор, Передаточні характеристики.