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Optimized design and investigation of novel reversible toffoli and peres gates using QCA techniques

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ABSTRACT

The QCA is a revolutionary dominating transistor-less computational nanotechnology based on quantum dots. As such, it might be used in the next generation of quantum computational nano-electronics devices. New molecular materials like QCA are being developed for use in nanoscale devices and cables. The major objective of this research is to optimize the design and investigate numerous properties of a QCA reversible logic circuit design. These locations include, limited Toffoli Gate (TG) and Peres Gate (PG). To address the key problems associated with the physical integration of digital circuits is power consumption and power dissipation which leads to synchronization issues, this research proposes a novel reversible logic gates (RLG-TG) a single layer coplanar approach. RLG designs with minimal design area, latency, and quantum cell count (QCA) are given and implemented using a Bijection functional method. Using the QD-E (Energy) tool, the first-order energy dissipation of the proposed shape and the impact of output bias cell temperature are also investigated. The proposed circuit designs were tested using the CVSE parameters, which had high clock signal saturation energies of 9.8e-22 d (Jules), recovery times for damping factors of 1e-15 s, and relative dielectric constants of 12.90 for GaAs and AlGaAs. The number of quantum cells used by the described new RLG-TG and RLG-PG designs is decreased by 38.23 % and 21.14 %, respectively, when compared to the optimal RLG designs employed in the state-of-the-art RLG designs. In this investigation of the proposed four-bit EPG and OPG circuits occupies 18.91 % and 38.27 % less design area, requires 46.15 % and 46.25 % less number of cells, and both designs has been 66.66 % improvement in delay.

1. Introduction

The QCA is cutting edge new technology in the field of computational nano-communication. Nowadays, novel quantum-dots based QCA nanotechnology is more popular for designing of digital and computational circuits at nanometer (nm) scale. It has many advantages such as the smaller size of circuits in nm^2, low power dissipation, faster-switching speed in terahertz [1,2]. The emerging QCA nanotechnology concept is based on bi-stable cellular automata. The idea of QCA was first introduced in 1993 by Lent, C.S. et al. [3] The quantum cellular automata nano-technology have needs for nanoelectronics devices and circuits for computing, automotive, entertainment, communication and other applications, with advancement as well as improvements in terms of high-speed, fast data transmission, low delay, minimum design area, and ultra-power consumption [4].

Quantum electronics based several computing devices and digital logic gates are implemented in the last decade. With the Shannon-Von-Neumann-Landauer (SNL) equation included in the equation, this is reasonable. (1) to account for the energy (Ebit) needed to transmit binary data.

$$E_{(Energy-bit)} \geq E_{SNL} = K_b T \ln 2 \quad (1)$$

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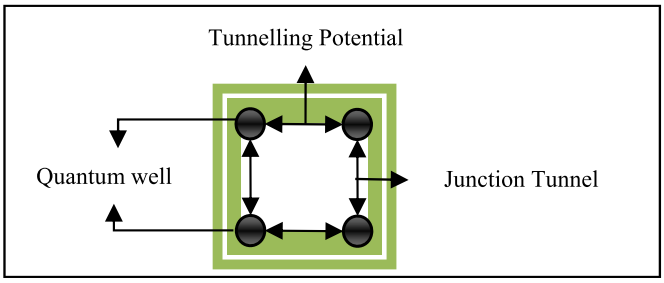

Fig. 1. QCA cell based on Quantum dots.

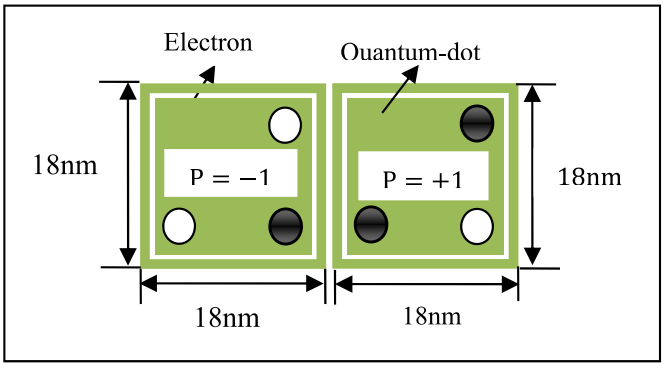

Fig. 2. Polarization of QCA cell.

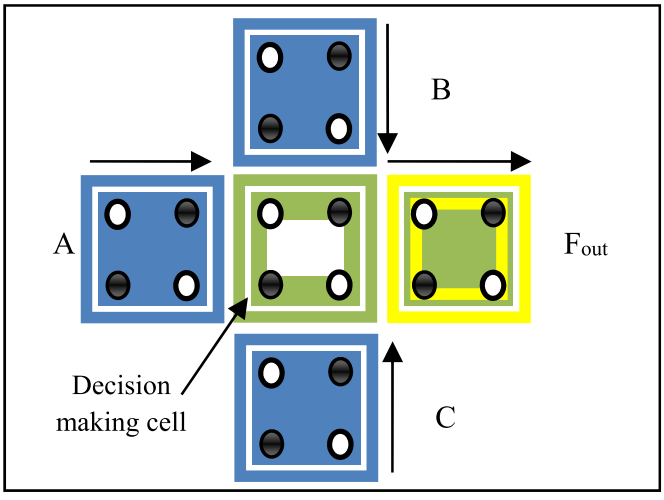

Fig. 3. QCA gate Maximization.

Several semiconductor materials with lattice mismatch, such as InAs/GaAs, are used in the fabrication of quantum dots. Strain is introduced at the interface between the two materials during monolayer-scale Molecular-Beam-Epitaxy (MBE) growth of InAs on GaAs. The relative permittivity of the material used in simulation is 12.9 for GaAS/AlGaAS. The QCA technology operates on room temperature and high device density up to 10^{14} device/cm^2 as compared to traditional CMOS technology. Therefore, from a functional point of view, QCA operation places three very high demands on molecules. The stability of quantum-dot geometry, synchronized clocking, and charge confinement are the three most important factors. High-dot-density, an anisotropic nano-structure, and uniform-dot sets with well-defined patterns are only a few of the distinguishing characteristics of quantum-dot molecules. Droplet epitaxy may be used to make quantum rings in InP and InAs. The QD-E (Energy) tool was used to confirm the

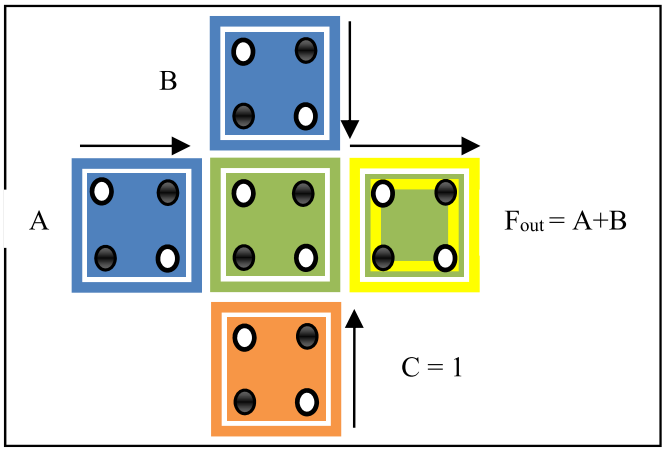

Fig. 4. QCA-OR-logic (QOL).

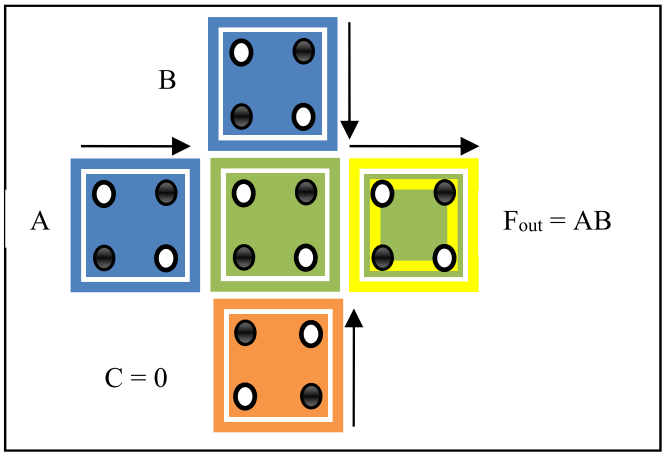

Fig. 5. QCA-AND-logic (QAL).

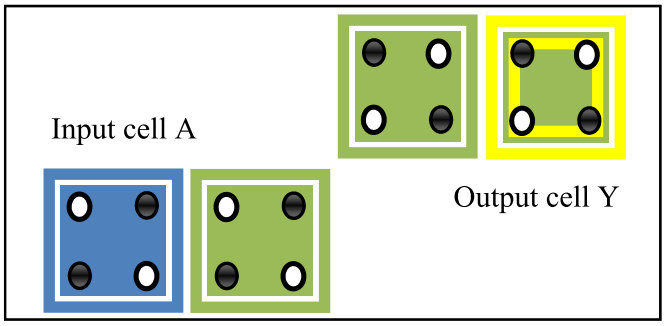

Fig. 6. Inverter for the QCA

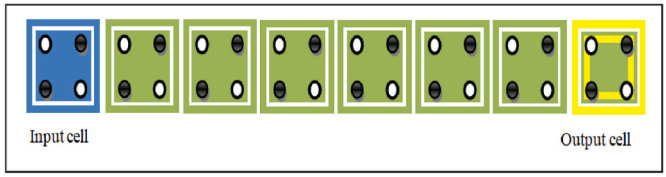

Fig. 7. Quantum dots based on wire (phase = 900).

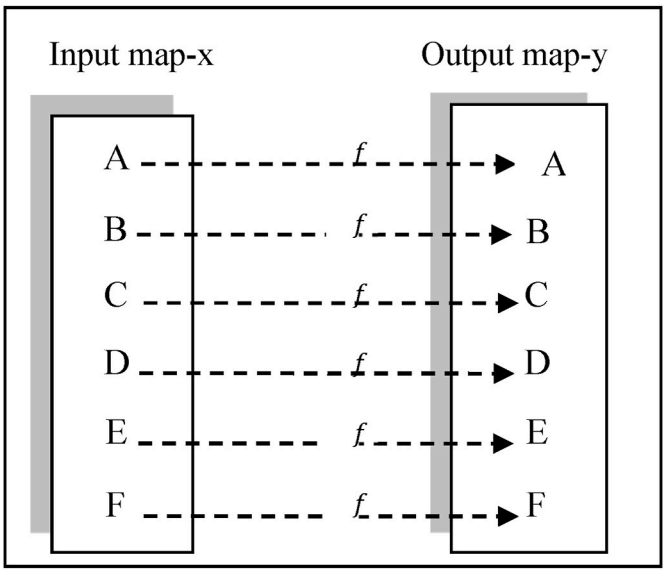

Fig. 8. The bijective functional mapping.

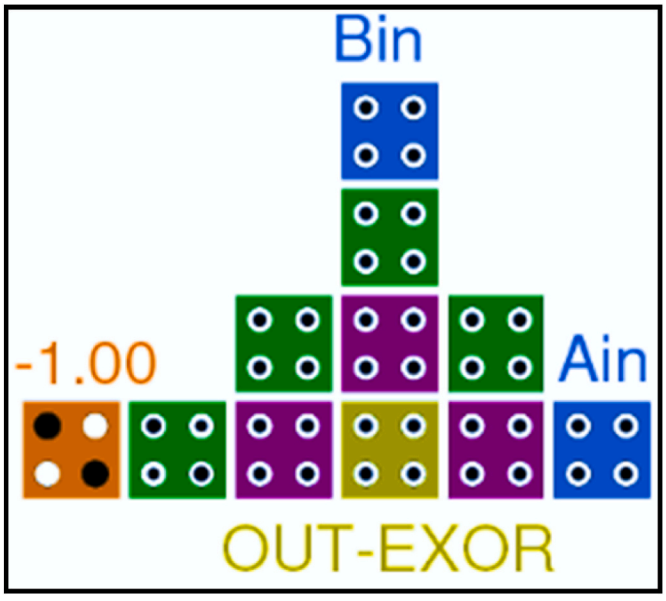

Fig. 9(a). QCA-EXOR logic gate design.

optimal energy dissipation as well as the cell temperature effect that biases the output of the proposed structure. To resolve these shortcomings, a novel single layer coplanar method is proposed to solve the power consumption, power dissipation and the synchronization issues. The main contributions of the proposed method are presented below.

- In this research, a novel single layer coplanar method has been used which will provide a solution for RLG-TG and RLG-PG that requires less overall design space and assures minimum clock-cycle delay.
- A functional parallel technique is used to implement the provided reversible logic gate (RLG) layout designs in order to decrease the quantity of QCA (quantum) cells, latency, and minimal design area.
- A single layer Nano computing architecture of even and odd parity generators around QCA technology using the QCA Designer-E tool with a synchronized clocking is developed using extremely ultra-power efficient and has a power dissipated of less than 1.5 nW.
- The performance of the proposed method is evaluated by using power consumption, energy dissipation and gate counts.
- Calculated the energy consumption by the design using the novel QCA Designer-E tool for TG and PG circuits.
- Performance analysis has been compared with existing designs in terms of cell count, design area, and delay using synchronous clocking zone.

Section 2 of this study is devoted to a review of the relevant literature. In this section, we will discuss the QCA layout that is part of the planned work. The materials and techniques are described in Section 3, followed by the findings and discussion in Section 4, and finally the conclusions in Section 5.

2. Review of related work

Nowadays, the design of different logic gates and circuits is designed by QCA technology using quantum electronics concepts. This technology is the mostly preferred in research area by researchers for building efficient QCA devices because this technology are a modern transistorless nano-computational exemplification in nano-technology. It uses the charge arrangement between quantum dots to encode binary information, making it possible to simulate the structure of the QCA quickly and determine its function quickly.

The QCA designs of XOR and XNOR logic gate using majority gate, wire and inverter have been proposed in various articles [5,6]. Bhoi, B [14]. built an RLG based entirely on three-bit parity protection, and these circuits were created using 27 QCA cells with an occupied region of 0.06 m2. Kumar, D. et al. [4] have been designs 3-bit even and odd PG. The both EPG and OPG designs consist of 49 QCA cells, utilized design area of 0.04 μm^2 without any crossover and obtain 0.75 clock cycles delay. Das, J.C. et al. [7,8] have been proposed coplanar reversible nano-communication system having three section first parity generators, second transmission media and last section is parity checker circuits. The ROPG and checker circuits consists of 72 and 130 cells, utilized design area of 0.078 μm^2 and 0.0143 μm^2 and incur same clocking zones four. By using a number of gate with three inputs and an inverter, Khankpour M. et al. [4] developed a brand-new multi-layer parity generator structure based on QCA. The clock cycle delay of the suggested device, which employs 86 QCA cells, is 0.75. Design and simulation of a four-bit even parity occupies design area is 0.1 μm^2, 87 QCA cells and 1.75 clock cycles delay by Singh, G. et al. [9,10].

The authors Chen, H et al. [11], have presented "XOR-gates" designed using 9 cells and a latency of 0.25 clock cycles. They found a maximum polarization of +9.65e-001 and a minimum polarization of −9.30e-001, although the designs by Chen, H. et al. present [12] have smaller output variation than the suggested design. In the layout of XOR gate designed by Ref. [13], the output polarization is completely depending on fixed polarization cell (P = −1), which is closest to the output cell. So, the presented design in Ref. [13] has less-fault tolerant.

Majeed, A.H. et al. [14] developed a 2-entry XOR gate in 2018 with a delay of under 0.25 clock cycles using nine QCA cells. They have used the same methodology, only the positions of cells have been modified to show the novelty. The layout has the same issue of the fault tolerant, due to maximum dependency on single static polarized cell. The presented QCA layout of XOR gate by Majeed, A.H. et al. [15] has the same number of cells as given by Chen, H. et al. [16], but the QCA layout is different.

An RLG gate mapping (Toffoli, NOT, Feynman, Peres, and Fredkin)-based heuristic function approach was introduced by M. A. Shafi et al. [17]. QCA reversible channel routing based on Fredkin, PG, and TG reversible gates was suggested by J. C. Das et al. [18]. Its AOP is maximized between 1K and 10K. QCA cells 114 and 136 are used for the reversible TG and PG, and their design areas are 0.143 μm^2 and 0.176 μm^2 with latencies. The results showed that for Feynman, the latency was 0.5, the design area was 0.016 μm^2, and the cell count was 23, while for Toffoli and PG, the related values were 0.75, 0.034 μm^2, and 34,

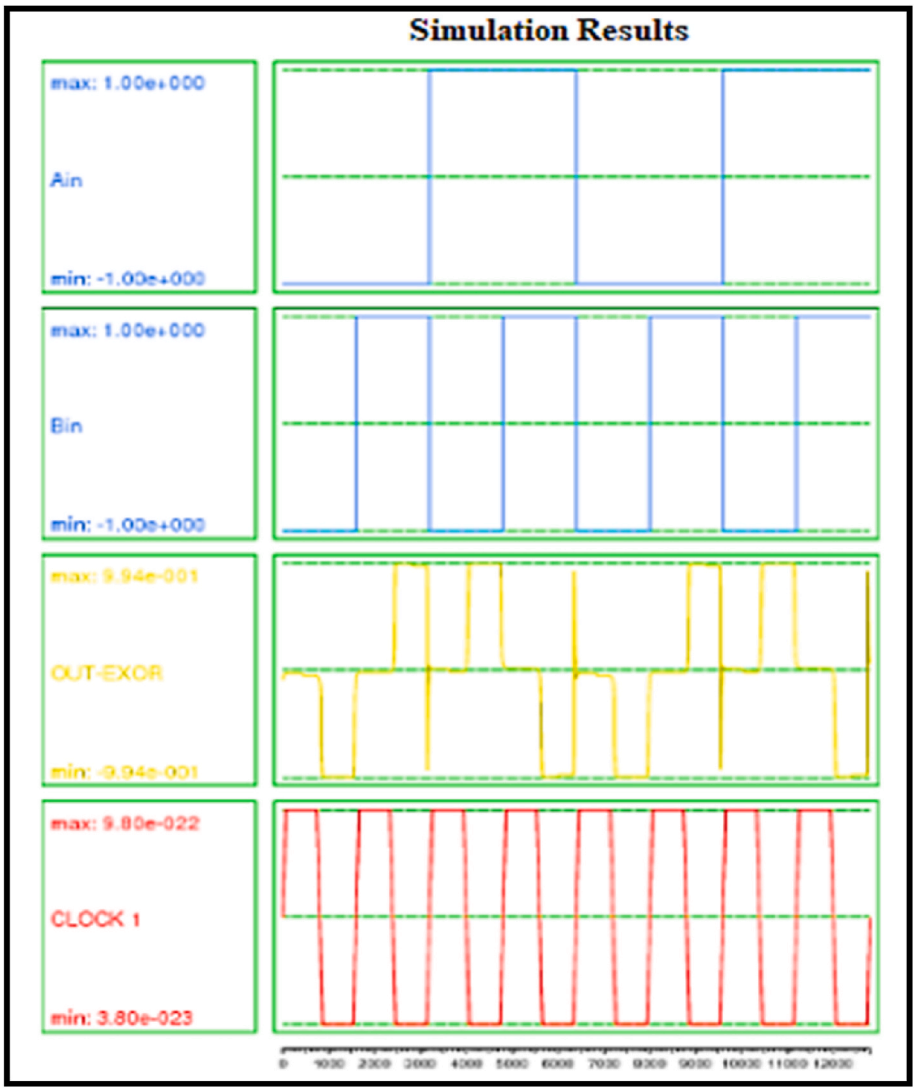

Fig. 9(b). Output performance of QCA-EXOR logic.

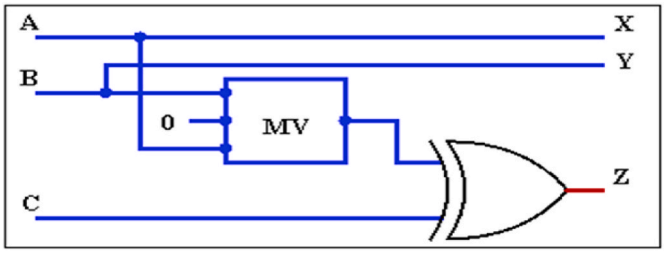

Fig. 10. Logical diagram based on toffoli gate.

respectively. A variety of reversible logic gates that are based on QCA 5-input majority voter logic were described by G. Singh et al. [19].

M. Kianpour et al. [20] present a combinational complete adder/-subtractor RLG with Toffoli gate that has a capacity of 8 bits. Their work is predicated on Landauer theory. QCADesigner is used to create both circuits while running approximation simulations in a "bistable" fashion. C. Mukherjee [21] used the LTEx module to create a Toffoli gate (33), which consisted of 36 quantum cells and took up a total of 0.0388 μm^2 of space in the design. The XOR-logic and PG reversible logic suggested by A. Sarker et al. [22] made use of 99 quantum cells, 0.1008 μm^2 cell area, and 4 clocks.

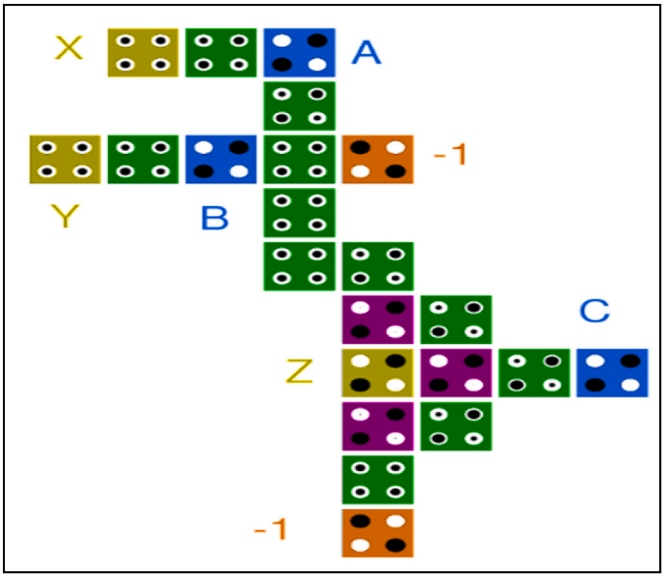

Fig. 11. QCA design for (3 × 3) Reversible Logic Gate with Toffili Gate.

Fig. 12. Output based on RLG-TG (3 × 3).

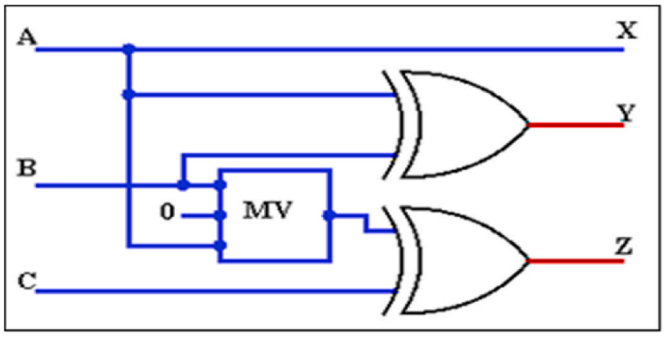

Fig. 13. Logical diagram for (3 × 3) Peres gate (PG).

The working of inter-dot barrier for clocking is following.

1. Slowly raised inter-dot barrier during switch (definitive polarity).
2. Remain constant inter-dot barrier during the hold (completely polarized).
3. Starts reducing barrier potential during the release phase (moving from polarized state to un-polarized state).
4. No inter-dot potential barrier (becomes zero) during the relax (cell un-polarized).

The increased use of cells during build, the amount of majority gates, the classes employed during build, and the delay in clock cycles were all issues with earlier designs. This work aims to illustrate and investigate a number of QCA inverting logic circuit design's qualities. Inverter gates can be used to implement inverter circuits. These locations include, among others, Toffoli Gate (TG) and Peres Gate (PG). To address the physical layout design and synchronization issue, this research proposes

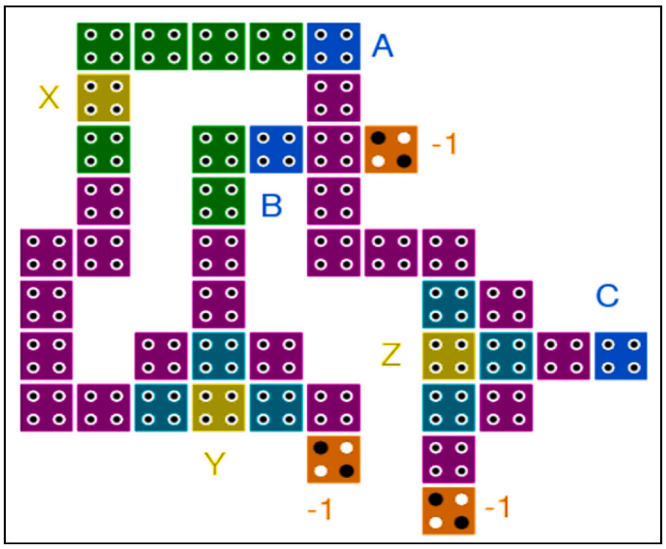

Fig. 14. QCA design of reversible logic gate with Peres gate (RLG-PG).

a single layer coplanar approach. Reversible logic gate (RLG) designs with minimal design area, latency, and quantum cell count (QCA) are given and implemented using a Bijection functional method.

3. Proposed methodology

In this paper, a novel single layer coplanar method is proposed to solve this physical layout design and synchronization problem. The presented reversible logic gate (RLG) layout designs are implemented by a Bijection functional algorithm for reduction of the number of QCA (quantum) cells, latency, and minimum design area.

3.1. Fundamental of QCA-design technology

A "quantum cell" serves as the fundamental constituent of a QCA, as can be seen in Fig. 1. It is made up of four quantum dots that are laid out in a square and connected to one another by tunnel barriers as well as a vertical capacitor [9]. As can be seen in Fig. 2, the polarization states P = +1 and P = −1 in the quantum cell (also known as a QCA cell) correspond to the logic 1 and logic 0 values, respectively. One of the most important aspects of the way quantum computers process data is the use of digital logic gates that can handle two quantum bits, also known as qubits [23]. Coulomb (C) interactions and electrostatic force are used to transmit information between neighboring quantum cells. The cellular level In Eq. (2), we define cellular polarizations (P).

$$P = \frac{(\rho_1 + \rho_3) - (\rho_2 + \rho_4)}{(\rho_1 + \rho_2 + \rho_3 + \rho_4)} \tag{2}$$

Fig. 3 depicts the three fundamental parts of the single cell offset, which is utilized to create all QCA logic gates from a single QCA cell. These elements consist of a majority voter, an inverter, and a wire. The logical process that MAJ-3 represents may be represented by equation (3) [20]. The polarity of a single input must be adjusted to a fixed value of 1 (P = +1) or 0 (P = −1), respectively, for MG to implement the OR and AND logic operations of QCA. The majority OR gate's logic function is described by Eq. (4), while the majority while gate's logic function is represented by Eq. (5) [19]. Figs. 4 and 5 demonstrate the configuration designs for three-input QCA-AND-Logic (QAL) and three-input QCA-OR-Logic (QOL), respectively.

$$F(A, B, C)_{maj-3} = AB + BC + AC \tag{3}$$

$$F(A, B, 1)_{\text{QCA OR Logic function}} = A + B \tag{4}$$

$$F(A, B, 0)_{\text{QCA AND Logic function}} = A.B \tag{5}$$

In Fig. 6, we see the QCA inverter in action, inverting the inputs. The QCA inverter is a straightforward circuit that converts the input signal (AA) from zero to one using information sent from the left mobile device to the right mobile device. A chain circuit is formed by joining many QCA cells together in the collection. Fig. 7 [13] depicts the layout topology of a 900 QCA-wire. QCA circuits regulated by Landauer clocks follow a four-stage signal progression: switch, hold, relax and release [21–30]. Eq. (6) is used to compute the phases of wires, and if each phase has a phase shift of π/2, then the phase that is regarded to be the reference phase is φ_1 [14]. ($\varphi_1 = 0, \varnothing_2 = \pi/2, \varnothing_3 = \pi$, and $\varnothing_4 = 3\pi/2$).

$$\varphi_i = i \bullet \frac{\pi}{2} \text{ (where } i = 0, 1, 2, 3) \tag{6}$$

3.2. Bijective algorithm mapping

For the purpose of carrying out the particular operation of mapping one input (I) to one output (O), the RLG employs a bijective technique. The amount of output ports inside the two-dimensional set of rules mapping characteristic is equal to the quantity of enter ports, as shown in Fig. 8 which strongly implies that every bit of the input vector corresponds to one of the output ports [15]. $I_v = (I_1, I_2, I_3, I_4, I_5, \ldots\ldots\ldots\ldots, I_N)$, Output vector bits $O_v = (O_1, O_2, O_3, O_4, O_5, \ldots\ldots\ldots\ldots, O_N)$. In 1980, Toffoli presented the RLG to describe the one-of-a-kind combination of circuit inputs and outputs [3,15]. The function f in equation (7) is a one-to-one correspondence function, sometimes referred to as a two-element function, if and only if it has two elements and two elements (or both elements and a function).

$$f_{(\text{Bijective function})} : x \rightarrow y \tag{7}$$

3.3. Exclusive-OR design for RLG

Reversible Logic Gates (RLGs), error detection and parity checking circuits, Arithmetic and Logical Units (ALUs), and so on all make use of the two-input exclusive-OR logic gate. Conventional EXOR logic circuits do not require one-to-one mapping, but the inverting XOR gate must perform a one-to-one function with the same number of inputs and outputs. Various research articles suggest designs for XOR gates with the least possible complexity. In 2017 [16], 2018 [17], and 2019 [24], A.N. Bahar et al. presented the reversible XOR design. The waveform result of the output simulation is represented in Fig. 9(a) and (b) (see Fig. 10).

In Eq. (8), we see the mathematical functional equation of the EXOR gate.

$$\text{Output of EXOR} \Rightarrow Y(A_{in}, B_{in}) = A_{in} \bigoplus B_{in} \tag{8}$$

3.4. Proposed QCA toffoli and peres gate design using molecular materials

Implemented design carry out the operation in accordance with Coulomb interaction. The components of the proposed design are a majority gate, an XOR, and an inverter. One-to-one mapping, feedback-free operation, fan-out, low trash production, and constant inputs are only a few of RLG's useful operational qualities [18]. A total logic calculation (TLC) will be produced from equation (9), where the variables are, respectively, = 2-input exclusion OR logic gate, = 2-input AND logic gate, and = NOT active.

$$T = \alpha(EX - OR\ Logic) + \beta(AND\ logic) + \delta(NOT\ logic) \tag{9}$$

3.4.1. Toffoli logic gate (CC-NOT)

In Eq. (12) [25–28], the operation (CZ) is carried out via the Toffoli reversible logic output Z. Fig. 11 depicts the actual Tomasso-toffoli gate QCA architecture that was implemented. The 90° QCA cells that make up its architecture were based on one 3-input majority voter and 2-input

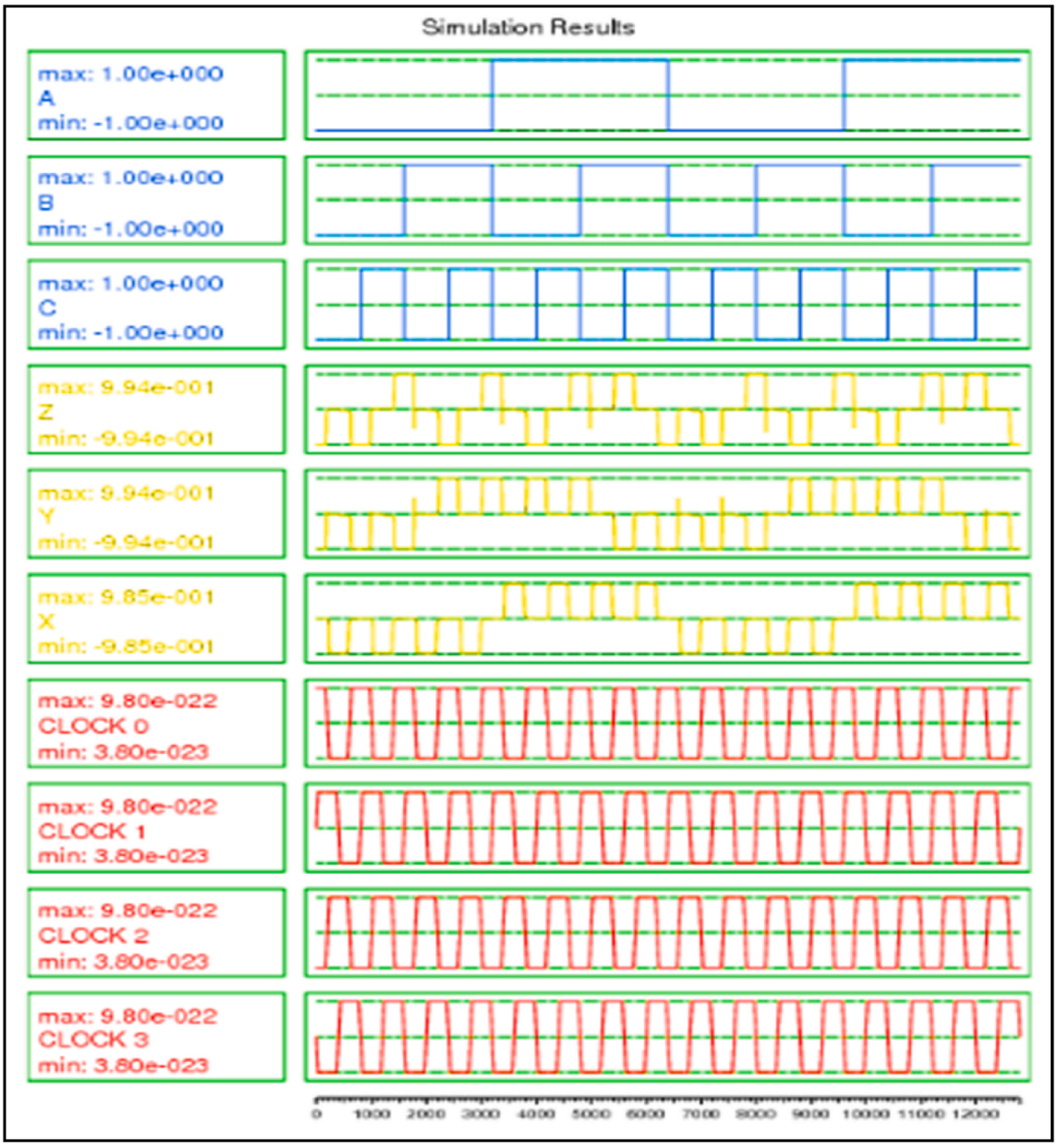

Fig. 15. Output based on RLG-PG (3 × 3).

XOR logic. The number of QCA cells utilized in this design is 21, the design area is 26524.10 nm2 = 0.03 m2, and the number of delays is 0.5. Fig. 12 display the validated simulation output findings.

$$A \leftrightarrow X = A \tag{10}$$

$$B \leftrightarrow Y = B \tag{11}$$

$$C \leftrightarrow Z = (AB) \oplus C \tag{12}$$

The majority voter Equation of toffoli gate is representing in Eq. (13)

$$Z = XOR(C, 0, M(A, B, 0)) \tag{13}$$

3.4.2. *Peres logic gate (PG)*

The RLG-PG gate (3x3) combines FG and TG operations. According to Eq. (9), the quantum-cost of PG is four [29,30]. Equations (14)–(16) provide a mapping function between input and output vectors. Fig. 13 depicts the logical block architecture, whereas Fig. 14 shows the QCA arrangement [29,30]. Using a coplanar single-layer architecture, the PG crammed 44 quantum cells into an area that measured 43710.75 nm2 = 0.043 m2. Peres gate (PG) output simulation results are shown in Fig. 15.

$$A \leftrightarrow X = A \tag{14}$$

$$B \leftrightarrow Y = A \oplus B \tag{15}$$

$$C \leftrightarrow Z = (AB) \oplus C \tag{16}$$

The majority voter Equation of peres gate is representing in Eq. (17).

$$Z = XOR(C, 0, M(A, B, 0)) \tag{17}$$

4. Result analysis

The QCA Designer application, using the Bistable simulation engine's default settings, has been used to develop the proposed RLG. The

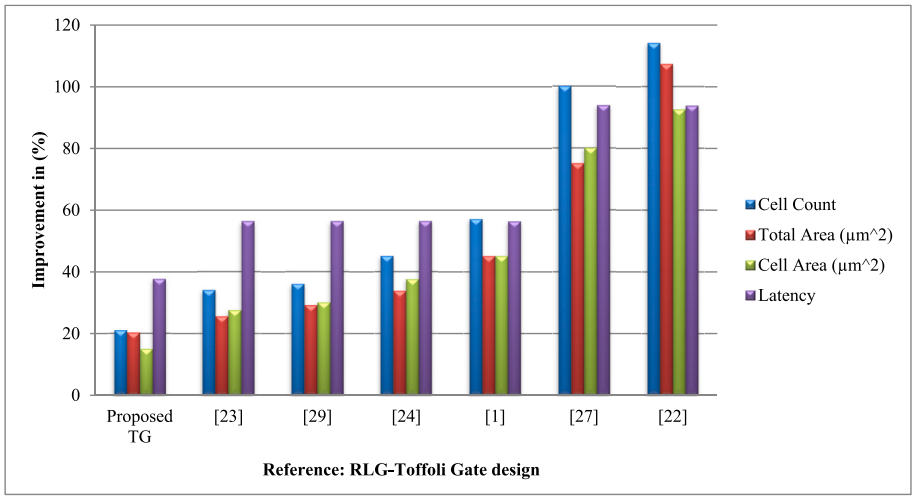

Fig. 16. Comparative output analysis between mentioned gates.

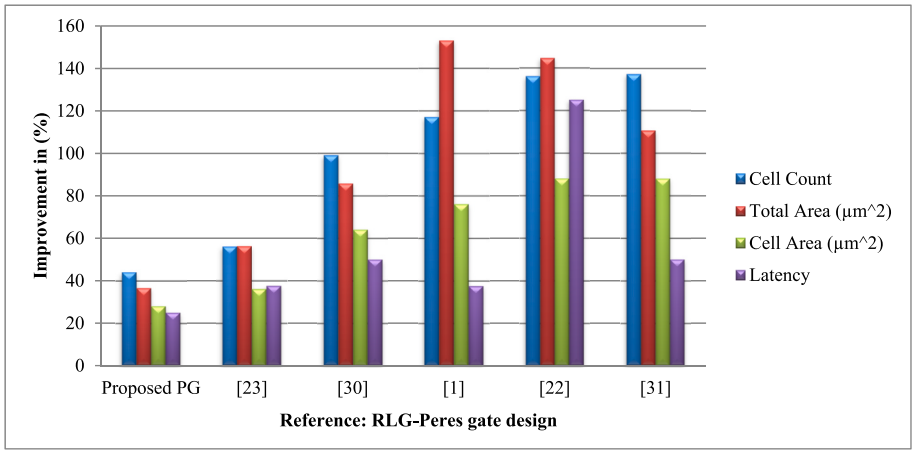

Fig. 17. Comparative output analysis with existing design.

default settings for the bistable approximation simulation engine are a layer separation of 11.5, a relative permittivity of 12.9 %, a relative permittivity of 12.9 %, a radius of effect of 65 nm and a convergence tolerance of 0.001,. Toffoli gate (RLG-TG) and peres gate (RLG-PG) circuits are designed using bijective algorithms in the RLG QCA architecture.

The number of quantum cells used by the described new RLG-TG and RLG-PG designs is decreased by 38.23 % and 21.14 %, respectively, when compared to the optimal RLG designs employed in the state-of-the-art RLG designs. This is the case because the suggested technology is able to accomplish this goal. Analyses of RLG-TG (toffoli gate) and current methods are shown in Fig. 16, and those of RLG-PG (Peres gate) are shown in Fig. 17. When compared to alternative methods, the suggested approach requires fewer cells, less space overall, and less time to complete [31–33] (see Fig. 18).

4.1. Energy dissipation calculation

K. Walus's unique QCA Designer-E version 2.2 tool [32,33] utility version 2.0.3 of the older QCADesigner program now comes in a designer edition. The Combined Vector Energy Tool (w/Energy), a different simulation tool accessible through the QD-E device, is used to calculate the amount of energy lost in eV. Using this beneficial resource, it is possible to calculate the amount of electricity lost inside the QCA circuit. Three distinct configurations of the simulation engine are offered in this tool: the coherence vector configuration, the coherence vector configuration (w/Energy), as well as the approximation using the bistable. A Hamiltonian matrix can be used to estimate the power and energy of the QCA cell for a two-state system, as shown in equation (18) [30].

$$H = \sum_{j} \begin{bmatrix} -\frac{1}{2} P_j E^k_{i,j} & -\gamma_i \\ -\gamma_i & \frac{1}{2} P_j E^k_{i,j} \end{bmatrix} \tag{18}$$

Using the QCADesigner-E tool and the linked vector simulation tool (with energy), we computed the overall energy loss resulting from the design. The proposed circuits account for relative dielectric constants 12.90 for GaAs and AlGaAs materials, relaxation periods for the damping coefficients of 1e-15 s, and high and low clock signal saturation energies of 9.8e-22 d (Jules) and 3.8e-23 d, respectively [32]. Input signal periods are 10e-12 s, simulation times are 80e-15 s, and the gap between iterations is 1e-17 s. For this computation, we used a single-layer design with a spacing between quantum cells of 20 nm, a quantum dot-diameter of 5 nm, and a standard QCA cell size of 18 nm by 18 nm. Eq. (19) demonstrates that the QCA mobileular's overall errors are zero over the full clock cycle of all active movements [33].

$$\text{Error} = E_{\text{bath}} - (E_{\text{clcok}} + E_{\text{IO}}) \tag{19}$$

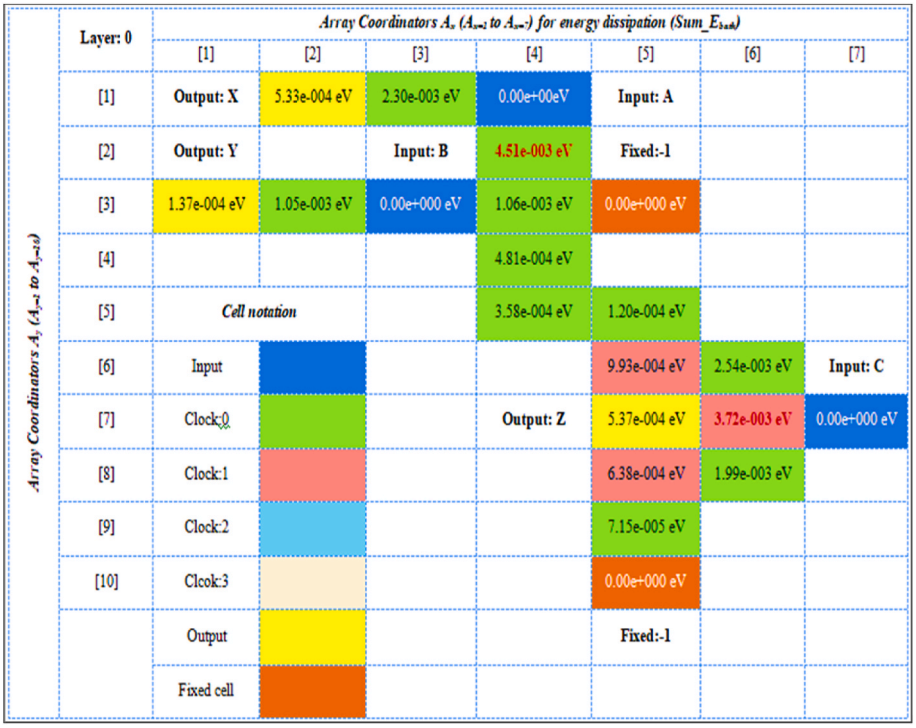

Fig. 18. Toffoli gate array-coordinates map for QCA Cell.

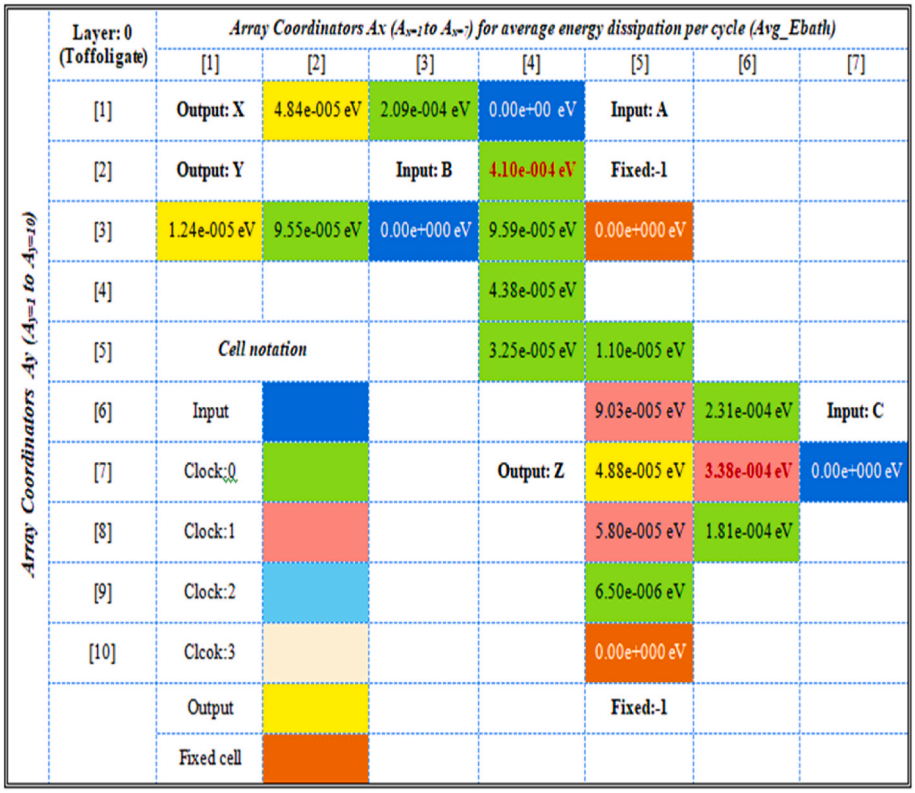

Fig. 19. Toffoli gate array-coordinates map for QCA cell average energy dissipation.

4.2. Array coordinates map for cell energy dissipation

In this section, we present our results for the RLG-TG and RLG-PG inverted good judgement gates at the community coordinate map (ACM) (see Fig. 19). Use the Consistency Vector Engine (w/Energy) configuration with the special QCADesigner-E (Energy) engine. Comparatively, 3.38e-004eV is equivalent to 0.338 meV, whereas 4.10e-004eV is equivalent to 0.41 meV. In QCA cells with fixed polarity (P = +1 and P = 1), it was discovered that the average energy loss via TG and PG was zero. This holds true for all input QCA cells. Figs. 20 and 21,

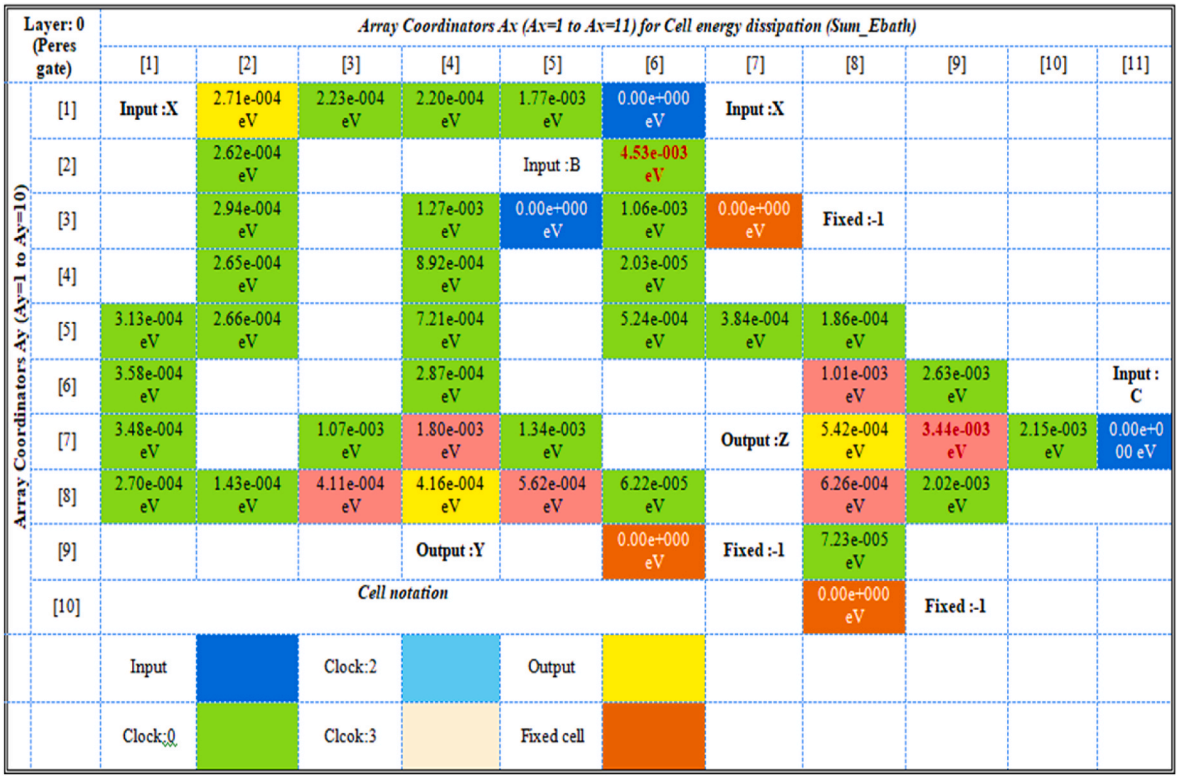

Fig. 20. Peres gate array-coordinates map for calculated QCA Cell.

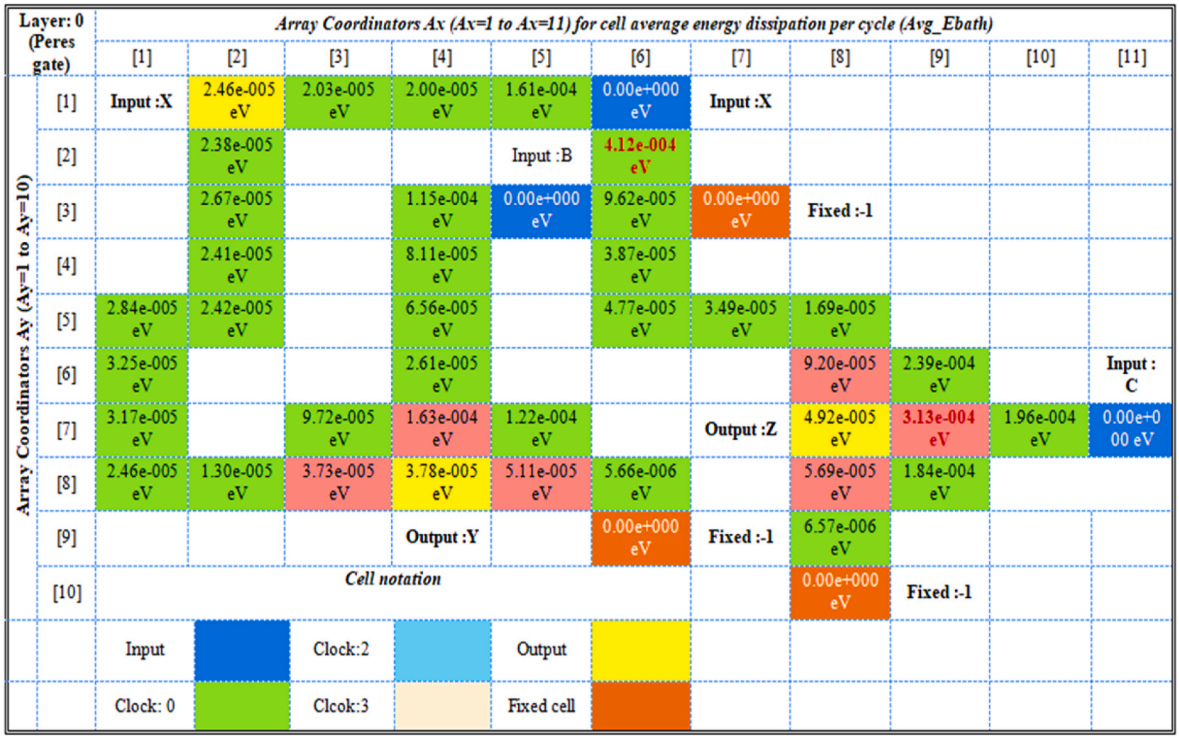

Fig. 21. Peres gate array-coordinates map for calculated QCA cell with energy dissipation.

respectively, display the lattice coordinate map for power dissipation and average power dissipation for the Peres gate [34,35].

To assess PRG's performance in relation to other reversing gates. The variety of current inverting ports, including CNOT, RQCA, RUG, as well as the advised TOFFOLI and PERES ports and Fig. 22, can be used to determine the number of ports necessary to carry out the usual functions. Compare suggested and reported retracements using a bar chart.

Quantum computing benefits from inverted gates' well-known low power and low latency characteristics. They are helpful in applications including microprocessors, DSP processors, and quantum computing

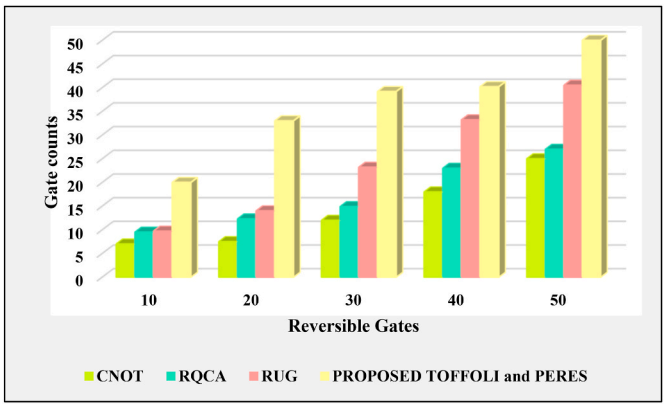

Fig. 22. Synthesis comparison using various reversible gates.

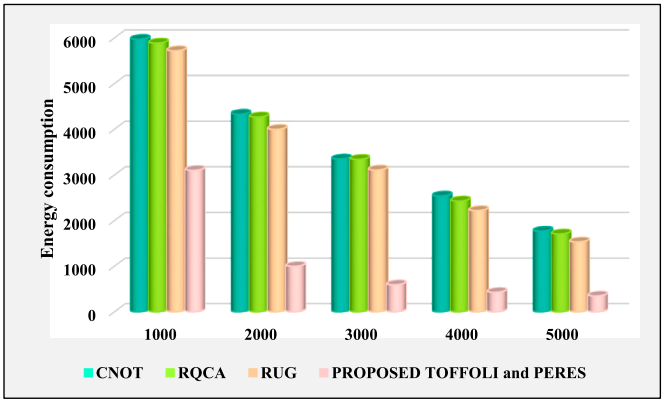

Fig. 23. Comparison of energy consumption.

due to their lower power consumption and faster functioning. Fig. 23 depicts the comparison of energy consumption using CNOT, RQCA, RUG and proposed TOFFOLI and PERES gates. The proposed TOFFOLI and PERES gates consumes less power consumption [36–38].

5. Conclusion

Using the software QCADesigner-E, the authors recommend building the reversible logic gates (RLG-TG and RLG-PG) on a coplanar single layer using a bijective functional method. This would be done using a bijective functional approach. In terms of overall cells, overall cells area, overall cells density, and latency, experiments have shown that the QCA-based layout is superior. The number of quantum cells used by the described new RLG-TG and RLG-PG designs is decreased by 38.23 % and 21.14 %, respectively, when compared to the optimal RLG designs employed in the state-of-the-art RLG designs. Using a coplanar single layer in QCA technology, Sasamal, T. N. et al. (2018) [23] provide a solution for RLG-TG and RLG-PG that requires 20.58 % and 34.84 % less overall design space, respectively, than earlier designs while still assuring minimum 0.5 clock-cycle delay. This study concludes by studying the power dissipation connected with the QCA-based efficient design of the RLG-TG and RLG-PG circuits, as well as the impact of temperature on the QCA or AOP of the cell output.

In this study, we developed an even and odd parity generator single-layer nanocomputing architecture based on QCA technology using the QCA Designer-E tool using a synchronized clock scheme. The presented circuits are extremely ultra-power efficient, having a power dissipated of less than 1.5 nW. In this investigation of the proposed four-bit EPG and OPG circuits occupies 18.91 % and 38.27 % less design area, requires 46.15 % and 46.25 % less number of cells, and both designs has been 66.66 % improvement in delay as compared to Mukherjee, C. et al. [39]. The proposed designs dissipate very less amount of energy at $\gamma = 1.0E_k$, such as 30.95, 30.99, 73.94, and 78.38 meV for 3-bit even, 3-bit odd, 4-bit even, and 4-bit odd PG circuits, respectively [40–42]. The presented circuits are based on the design of XOR gate. The XOR gate has distributed clocking among individual cells. In fabrication of such circuits, clocking to individual cells can be a challenge. Lithography techniques have more accurate in terms of placement of cells and clocking to overcome the limitations at nanoscale. In future, the fault tolerant and testability analysis can be done [43–45]. The proposed design of parity generator can be expanded and used as a module for designing other complex quantum dot based digital circuits.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability

No data was used for the research described in the article.

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